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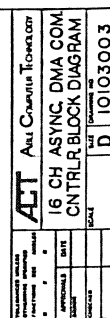
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	PROD. REL. PER E.O. 298	4-16-81	<i>[Signature]</i>

REF. ONLY

TOLERANCES UNLESS OTHERWISE SPECIFIED		ABLE COMPUTER TECHNOLOGY	
FRACTIONS	DEC	ANGLES	
±	±	±	
APPROVALS	DATE		
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CHECKED <i>[Signature]</i>	4-16-81		
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	B	10103003	
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NOT BE USED FOR DATA PATH PHRASES. IT IS THE RESPONSIBILITY OF THE USER TO ENSURE THAT THE DATA PATH PHRASES ARE USED IN THE APPROPRIATE MANNER. THE DATA PATH PHRASES ARE USED TO DEFINE THE DATA PATH OF THE PROGRAM. THE DATA PATH PHRASES ARE USED TO DEFINE THE DATA PATH OF THE PROGRAM. THE DATA PATH PHRASES ARE USED TO DEFINE THE DATA PATH OF THE PROGRAM.

2901 DATA PATH PHRASE										DBUS PHRASE										ORDER PHRASE										SEQUENCE CONTROL PHRASE									
D		+		S		C	A		B		D/S				LITERAL A				T		S		LIT B / RESUME DATA		AD														
DEST.		ALU		SOURCE		R	FILE		FILE		D DEST.		D SRCE.		ORDER		ADDR.		D	TEST		SEQ.	BRANCH		ADDRESS														
Q		R + S		A Q			Ø		Ø		DBUS		LITA		NULL		RO-DATA ERR URSET			-GOTO			LITB		Ø		Ø												
Ø	1	NOD	S - R	A	B	1	1	1	1	1	BRR	TPRM	REL_PIO	1	1	REL_PIO	WRT-DATA LED1 XNPR	1	1	-ALUZ	RETURN	1	1	1	1														
2	2	(BYPASS)	R - S	Ø	Q		2	2	2	2	DORL	MEM	SET_INTR			SET_INTR	RO-STAT LED2 XBRB			-ALUNEG	GOTO	2	2	2	2														
3	3	B	R OR S	Ø	B		3	3	3	3	DORU	MVR	RESUME			RESUME	N/A LED3 XBRA			-CRY	CALL	3	3	3	3														
4	4	BQ RIGHT	R AND S	Ø	A		4	4	4	4	MAR	ALU	NOT USED			NOT USED	RO-MODE NOT USED XMSYN			-DBIT	MAP_PIO	4	4	4	4														
5	5	B RIGHT	R AND S	D	A		5	5	5	5	UODR	UIDR	UART			UART	WRT-MODE EVNT1 NOT USED			-NO-DIAG	N/A	5	5	5	5														
6	6	BQ LEFT	R XOR S	D	Q		6	6	6	6	UAR	DIRL	A LATCH			A LATCH	RO-CMD EVNT2 NOT USED			-SSYN	VECTOR	6	6	6	6														
7	7	B LEFT	R XNOR S	D	Ø		7	7	7	7	MEM	DIRU	B LATCH			B LATCH	WRT-CMD DIAG NOT USED			-PB	N/A	7	7	7	7														
8	8						8	8	8	8	AORL					N/A				GOTO		8	8	8	8														
9	9						9	9	9	9	AORU					N/A				ALUZ		9	9	9	9														
A	A						10	10	10	10	AORX					N/A				ALUNEG		A	A	A	A														
B	B						11	11	11	11	NOT USED					N/A				CRY		B	B	B	B														
C	C						12	12	12	12	N/A					N/A				DBIT		C	C	C	C														
D	D						13	13	13	13	N/A					N/A				NO-DIAG		D	D	D	D														
E	E						14	14	14	14	N/A					N/A				SSYN		E	E	E	E														
F	F						15	15	15	15	N/A					N/A				PB		F	F	F	F														
47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72														

PRIORITY	EVENTS
7	PIO
6	DMAI
5	BRBI
4	BRBI
3	NOT USED
2	EVNT2
1	EVNT1
0	SCAN

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SHT	I	A	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D		
		E		
		F		
		H		
		J		
		K		
		L		
		M		
28	BUS-A21-L	N		
28	BUS-A20-L	P		
		R		
		S		
6	GND	T		
		U		
		V		

SHT	I	C	2	SHT
21	BUS-NPG-IN-H	A	+5V	6
21	BUS-NPGO-H	B	-15V	6
		C	GND	6
		D	BUS-D15-L	25
		E	BUS-D14-L	25
		F	BUS-D13-L	25
		H	BUS-D12-L	25
25	BUS-D11-L	J	BUS-D10-L	25
		K	BUS-D09-L	25
		L	BUS-D08-L	25
		M	BUS-D07-L	24
19	BUS-DCLO-L	N	BUS-D04-L	24
		P	BUS-D05-L	24
		R	BUS-D01-L	24
19	BUS-PB-L	S	BUS-D00-L	24
6	GND	T	BUS-D03-L	24
6	+15V	U	BUS-D02-L	24
		V	BUS-D06-L	24

SHT	I	E	2	SHT
		A	+5V	6
		B		
27	BUS-A12-L	C	GND	6
28	BUS-A17-L	D	BUS-A15-L	27
19	BUS-MSYN-L	E	BUS-A16-L	28
26	BUS-A02-L	F	BUS-C1-L	28
26	BUS-A01-L	H	BUS-A00-L	26
19	BUS-SSYN-L	J	BUS-CO-L	28
27	BUS-A14-L	K	BUS-A13-L	27
27	BUS-A11-L	L		
		M		
		N	BUS-A08-L	27
27	BUS-A10-L	P	BUS-A07-L	26
27	BUS-A09-L	R		
		S		
6	GND	T		
26	BUS-A06-L	U	BUS-A04-L	26
26	BUS-A05-L	V	BUS-A03-L	26

SHT	I	B	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D		
28	BUS-A19-L	E	BUS-A18-L	28
		F		
		H		
		J		
		K		
		L		
		M		
		N		
		P		
		R		
		S		
6	GND	T		
		U		
		V		

SHT	I	D	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D	BUS-BR7-L	21
		E	BUS-BR6-L	21
		F	BUS-BR5-L	21
		H	BUS-BR4-L	21
		J		
		K	BUS-BG7-IN-H	21
19	BUS-INIT-L	L	BUS-BG7-OUT-H	21
		M	BUS-BG6-IN-H	21
		N	BUS-BG6-OUT-H	21
		P	BUS-BG5-IN-H	21
		R	BUS-BG5-OUT-H	21
		S	BUS-BG4-IN-H	21
6	GND	T	BUS-BG4-OUT-H	21
		U		
		V		

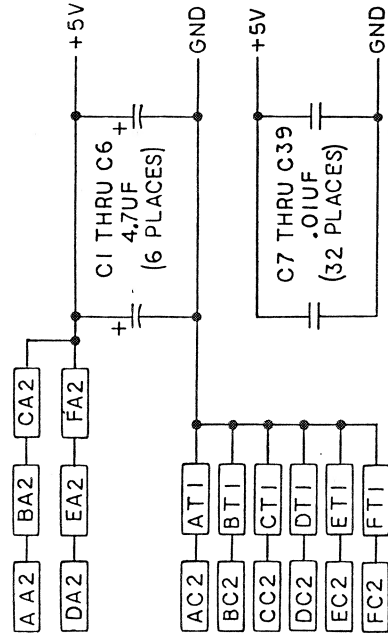
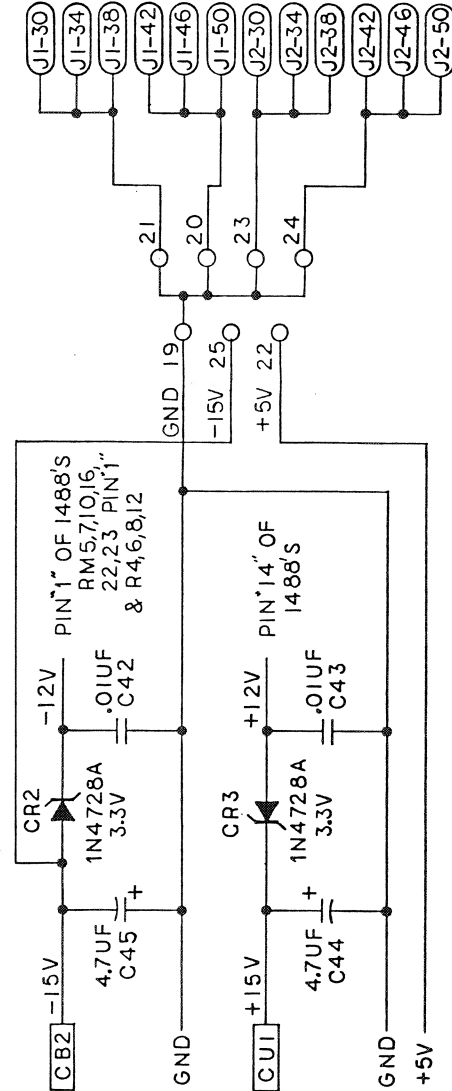
SHT	I	F	2	SHT
		A	+5V	6
		B		
		C	GND	6
19	BUS-BBSY-L	D		
		E		
		F		
		H		
19	BUS-NPR-L	J		
		K		
		L		
19	BUS-INTR-L	M		
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		P		
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		S		
6	GND	T	BUS-SACK-L	19
		U		
		V		

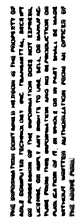
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SHT	J1	SHT
40 DTR00-H	1 2 CARRO0-H	38
40 DTR01-H	3 4 CARRO1-H	38
40 DTR02-H	5 6 CARRO2-H	38
40 DTR03-H	7 8 CARRO3-H	38
40 DTR04-H	9 10 CARRO4-H	38
40 DTR05-H	11 12 CARRO5-H	38
40 DTR06-H	13 14 CARRO6-H	38
40 DTR07-H	15 16 CARRO7-H	38
23 MAIN-H	17 18 GND	36
36 TXD00-H	19 20 RING00-H	39
37 RXD00-H	21 22 GND	36
36 TXD01-H	23 24 RING01-H	39
37 RXD01-H	25 26 GND	36
36 TXD02-H	27 28 RING02-H	39
37 RXD02-H	29 30 GND	6
36 TXD03-H	31 32 RING03-H	39
37 RXD03-H	33 34 GND	6
36 TXD04-H	35 36 RING04-H	39
37 RXD04-H	37 38 GND	6
36 TXD05-H	39 40 RING05-H	39
37 RXD05-H	41 42 GND	6
36 TXD06-H	43 44 RING06-H	39
37 RXD06-H	45 46 GND	6
36 TXD07-H	47 48 RING07-H	39
37 RXD07-H	49 50 GND	6

SHT	J2	SHT
40 DTR08-H	1 2 CARRO8-H	38
40 DTR09-H	3 4 CARRO9-H	38
40 DTR10-H	5 6 CARRIO-H	38
40 DTR11-H	7 8 CARRI1-H	38
40 DTR12-H	9 10 CARRI2-H	38
40 DTR13-H	11 12 CARRI3-H	38
40 DTR14-H	13 14 CARRI4-H	38
40 DTR15-H	15 16 CARRI5-H	38
36 GND	17 18 GND	36
36 TXD08-H	19 20 RING08-H	39
37 RXD08-H	21 22 GND	36
36 TXD09-H	23 24 RING09-H	39
37 RXD09-H	25 26 GND	36
36 TXD10-H	27 28 RING10-H	39
37 RXD10-H	29 30 GND	6
36 TXD11-H	31 32 RING11-H	39
37 RXD11-H	33 34 GND	6
36 TXD12-H	35 36 RING12-H	39
37 RXD12-H	37 38 GND	6
36 TXD13-H	39 40 RING13-H	39
37 RXD13-H	41 42 GND	6
36 TXD14-H	43 44 RING14-H	39
37 RXD14-H	45 46 GND	6
36 TXD15-H	47 48 RING15-H	39
37 RXD15-H	49 50 GND	6

SHT		J3		SHT
	GND	1 2	DB000-H	24
24	DB001-H	3 4	DB002-H	24
24	DB003-H	5 6	DB004-H	24
24	DB005-H	7 8	DB006-H	24
24	DB007-H	9 10	GND	
7	CS009-H	11 12		
	+5V	13 14	CS010-H	7
	GND	15 16	CS000-H	7
7	CS001-H	17 18	CS002-H	7
7	CS003-H	19 20	CS004-H	7
7	CS005-H	21 22	CS006-H	7
7	CS007-H	23 24	GND	
7	CS008-H	25 26	↑	
17	MINIT-L	27 28		
17	MDCLO-L	29 30		
17	CSTP-L	31 32	↓	
17	SYSCK-L	33 34	GND	
22	SSW1-L	35 36	SSW2-L	22
22	SSW3-L	37 38	CSS1-H	7
	+5V	39 40	+5V	

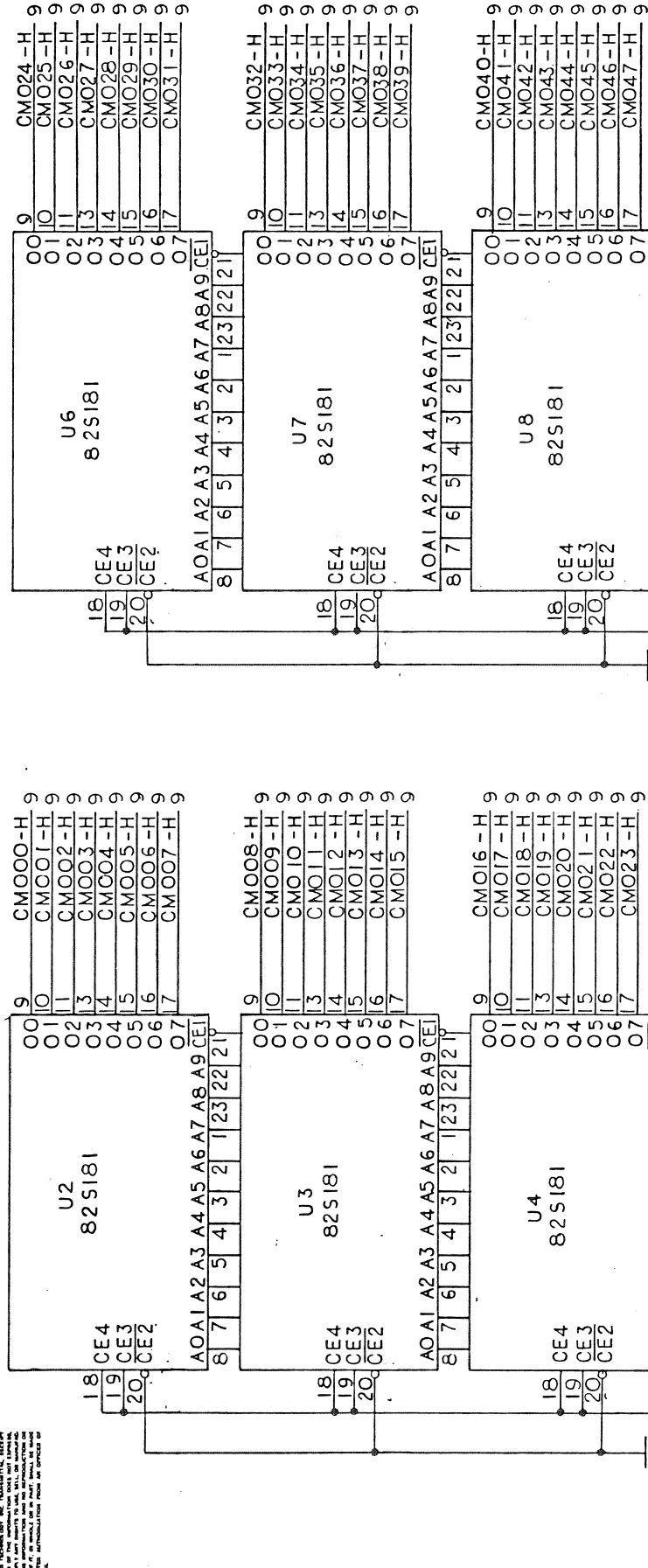




SI	SO	OPERATION
0	0	INCREMENT
0	1	NOT IMPLEMENTED
1	0	RETURN
1	1	GOTO/MAP/CALL /VECTOR

## CONTROL SEQUENCER

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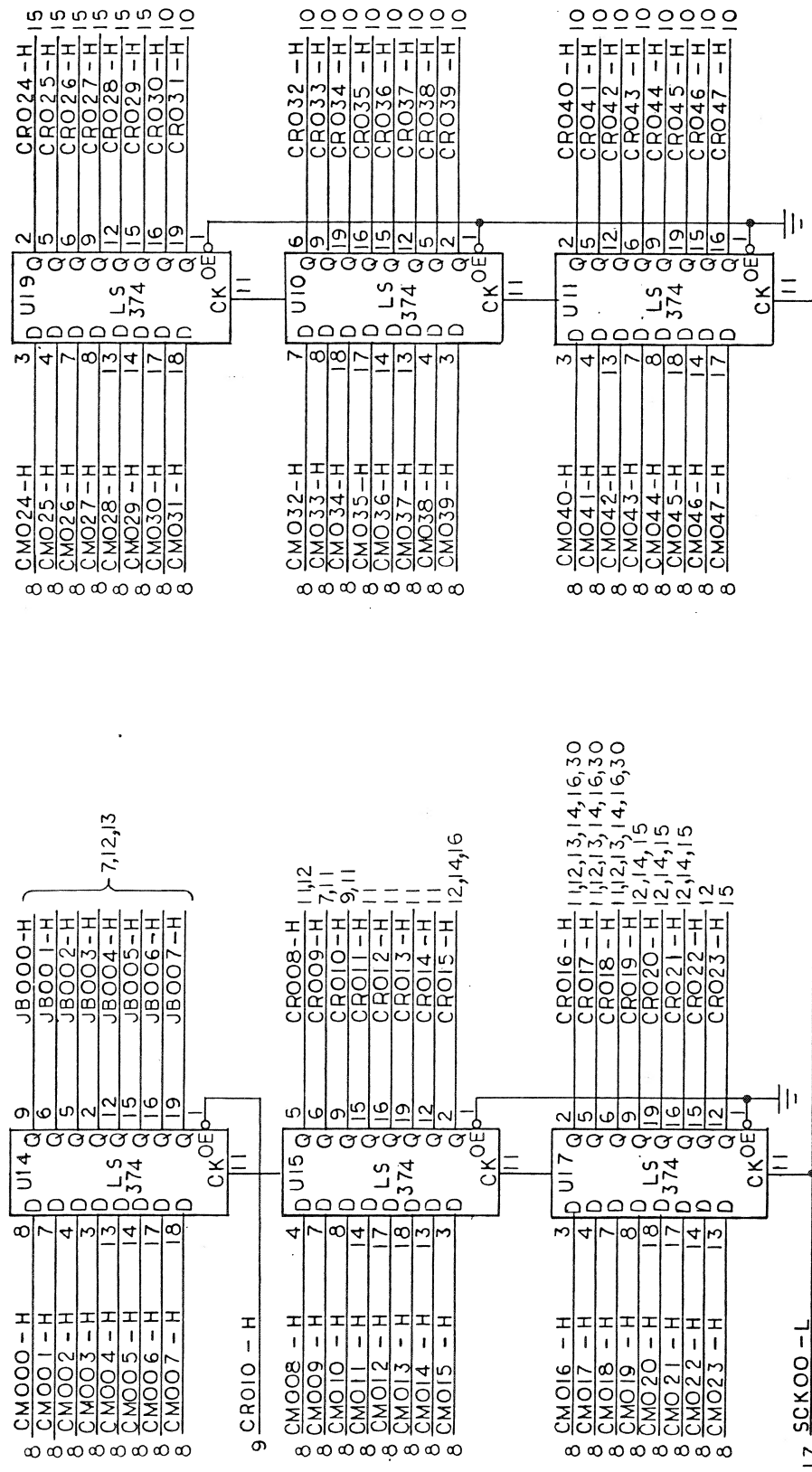


+5V R1 1K

CONTROL MEMORY

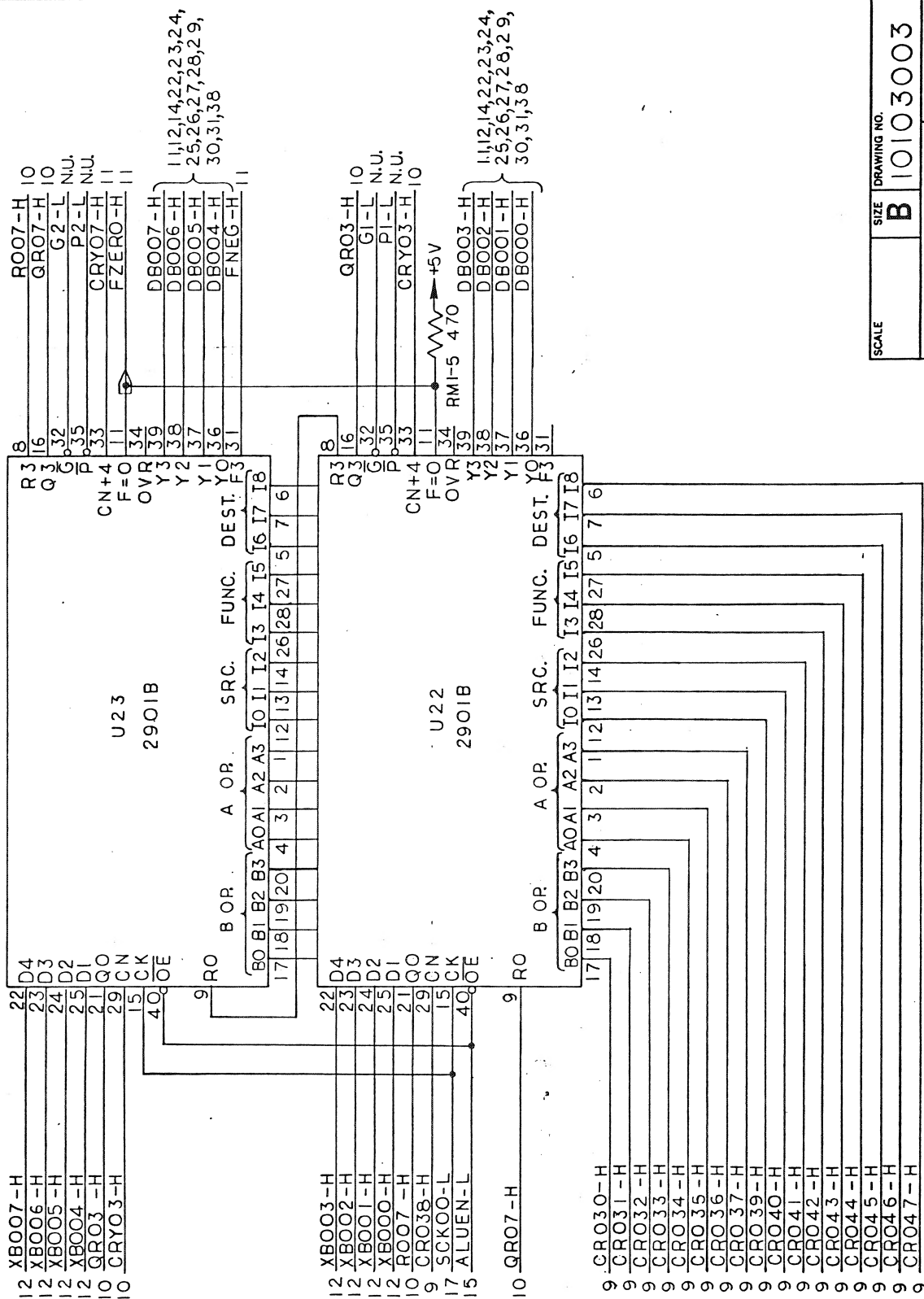


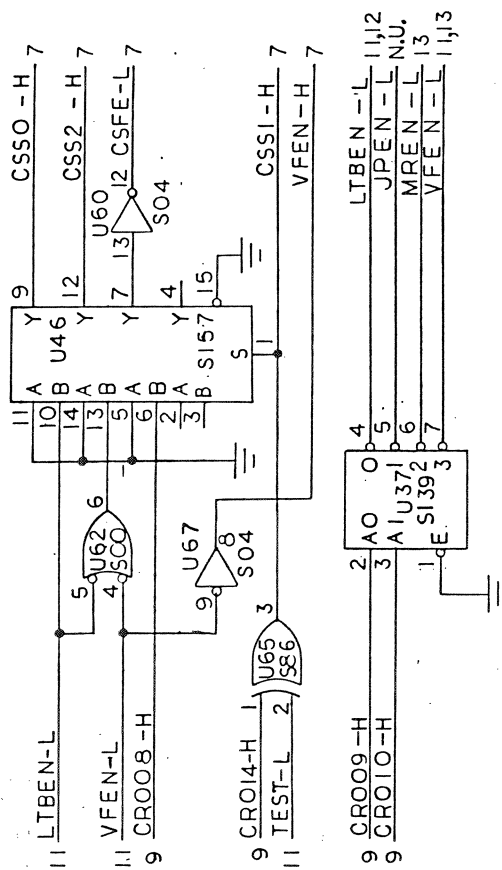
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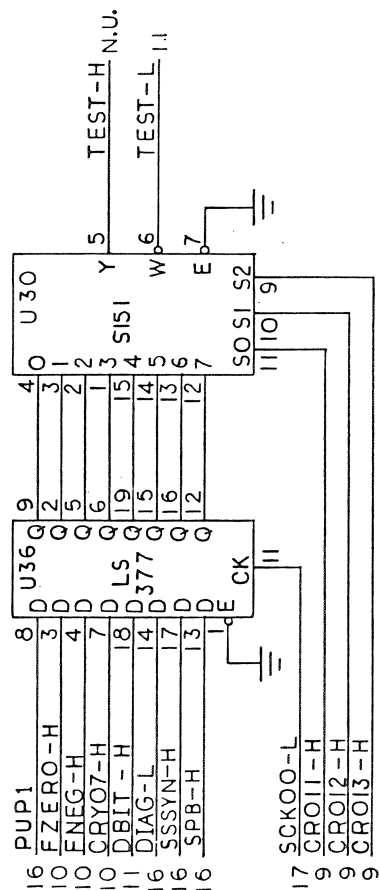
# CONTROL REGISTER

MICROPROCESSOR

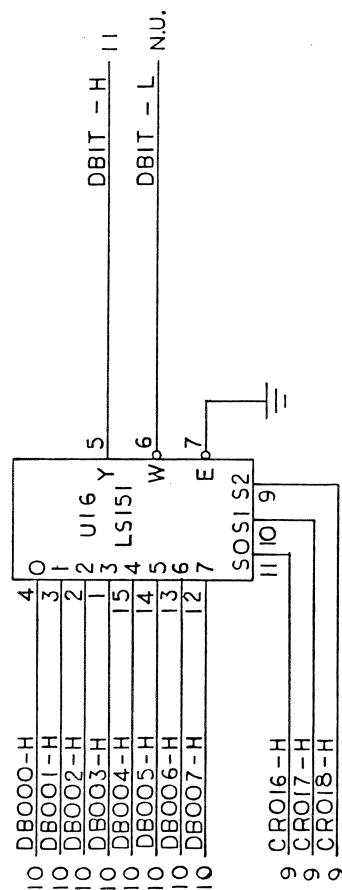




# SEQUENCE CONTROL



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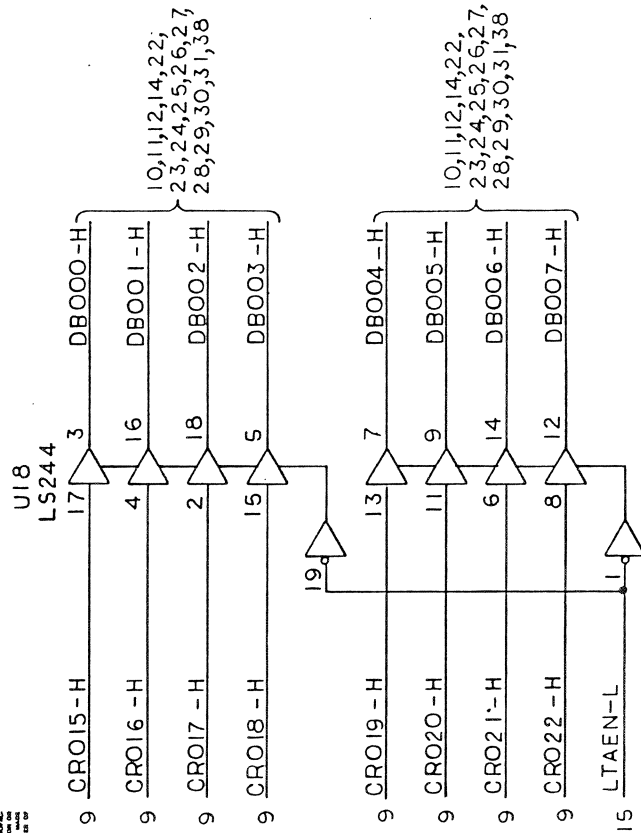


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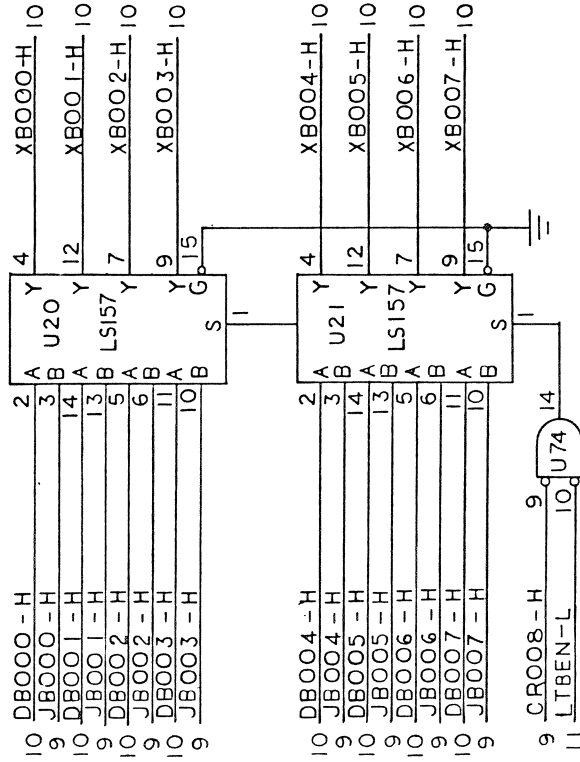
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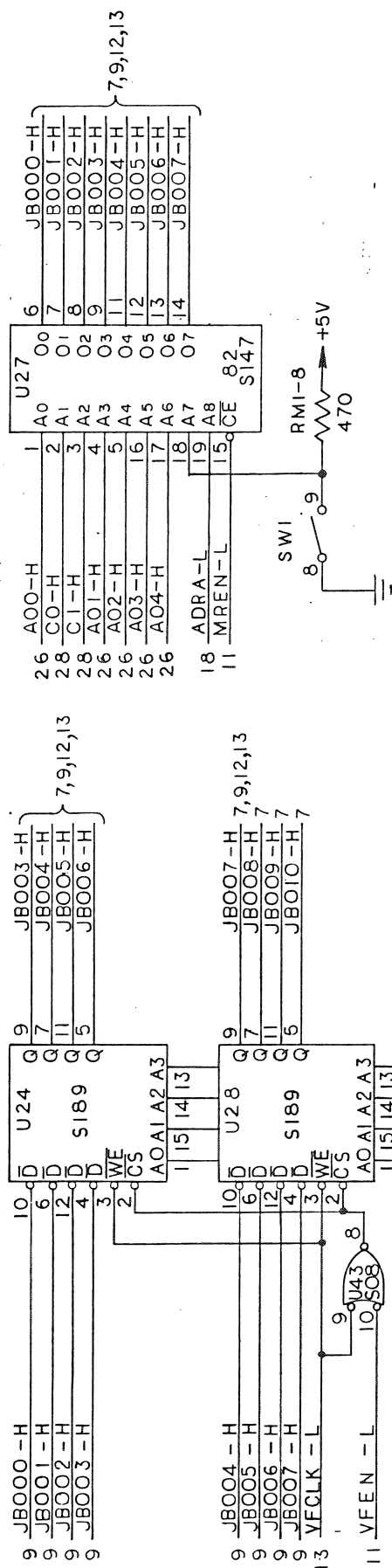
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LITERAL A

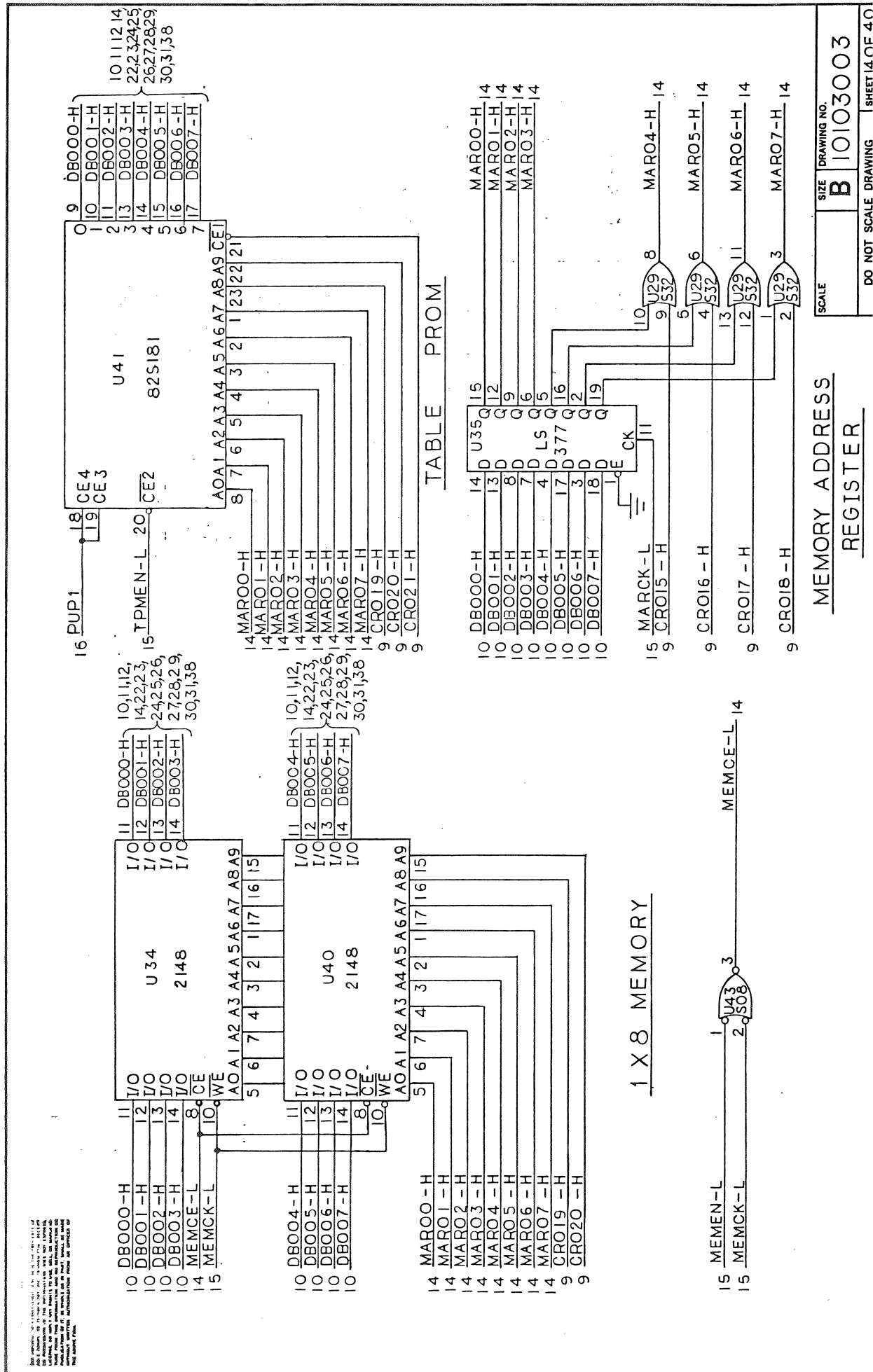


LITERAL B MUX

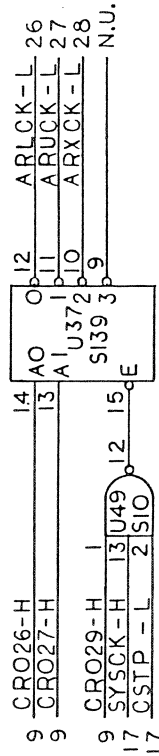
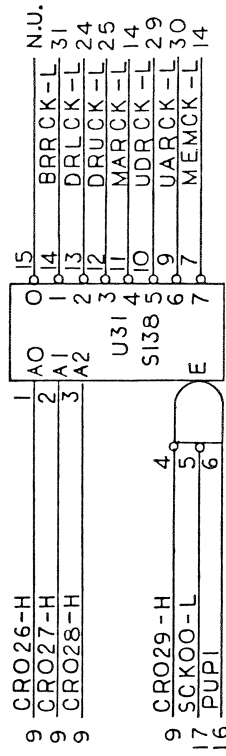


MAP · PROM

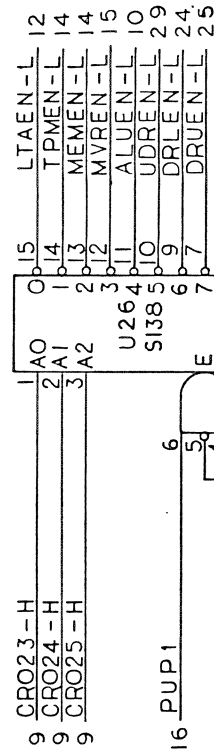
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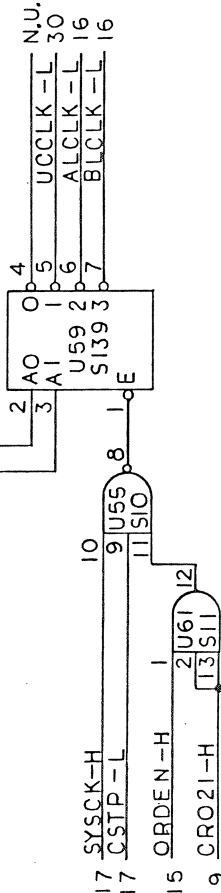
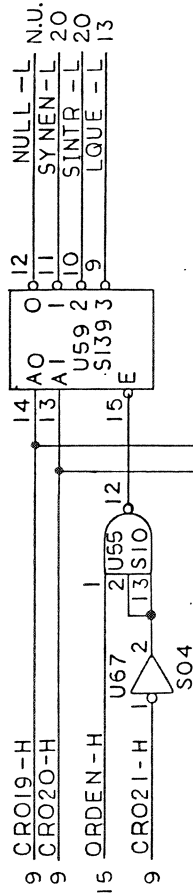
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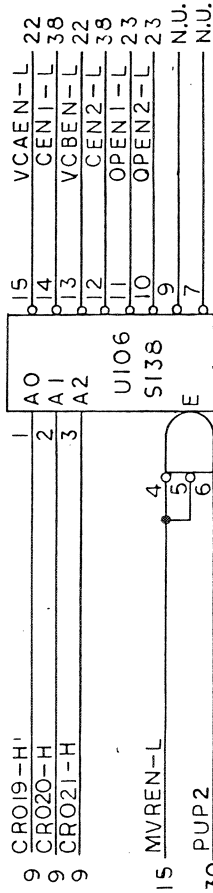
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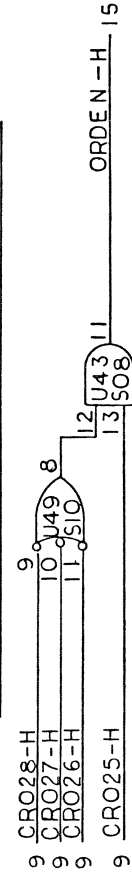
### SOURCE ENABLES



### ORDER DECODE



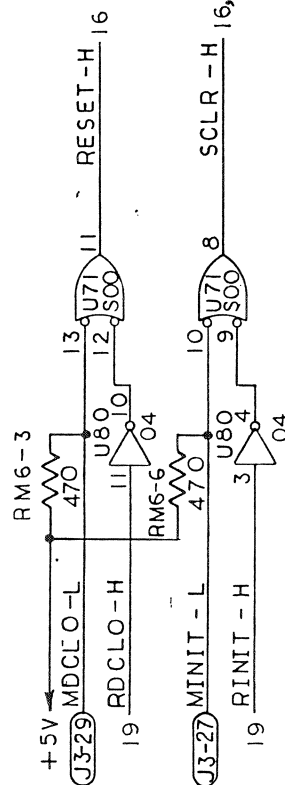
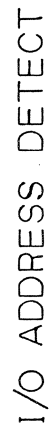
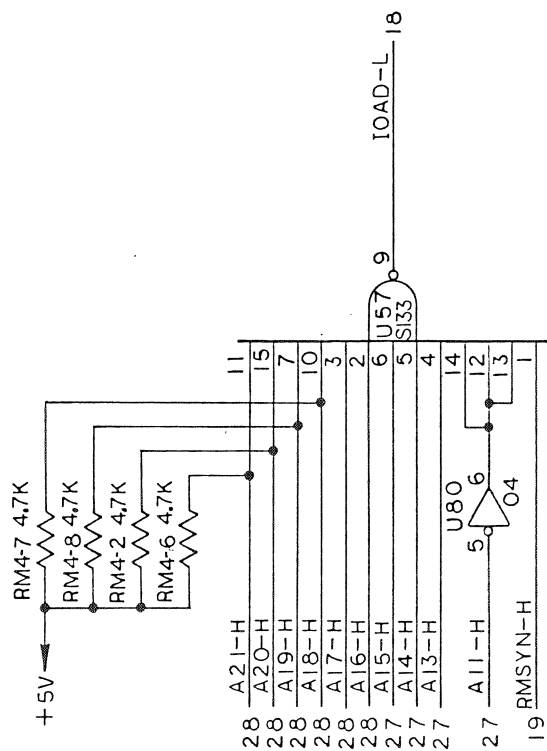
### VECTOR AND CARRIER ENABLES



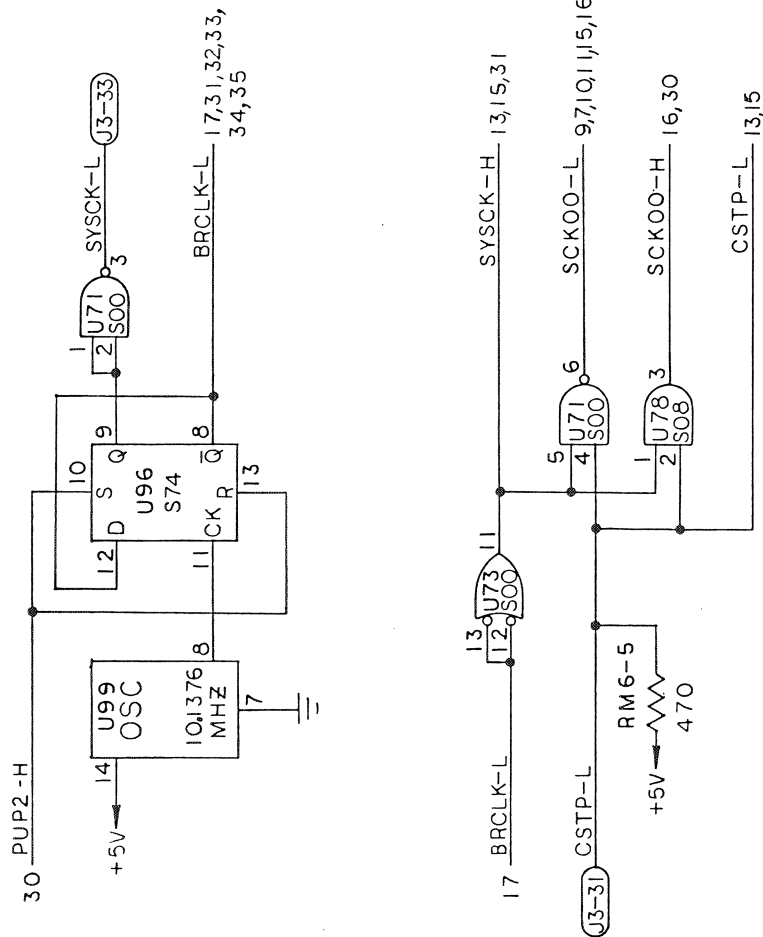
### ORDER ENABLE





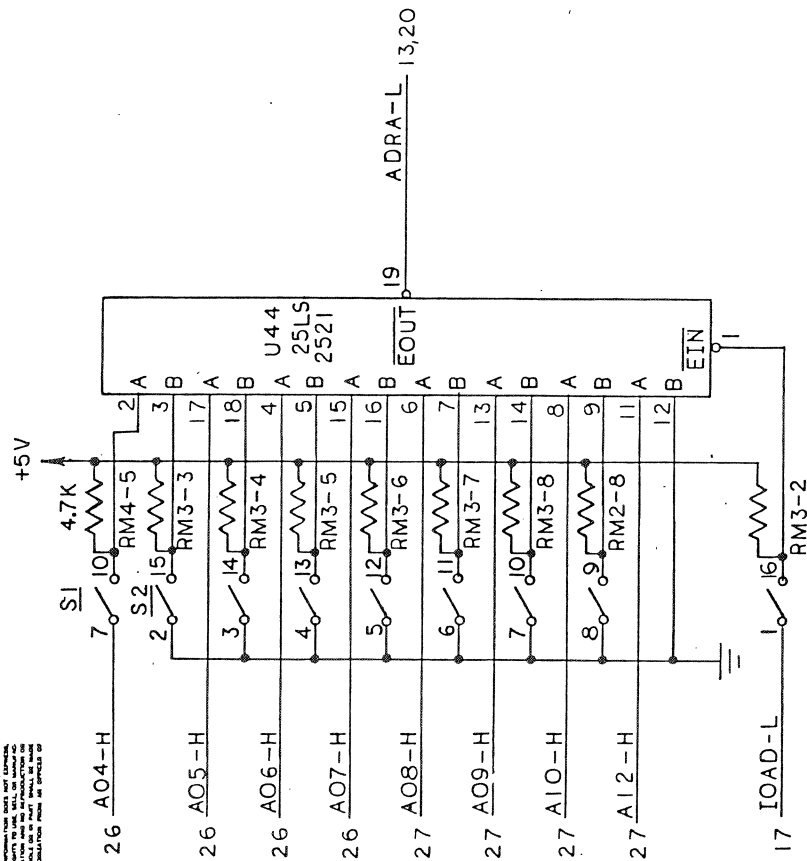


RESET AND SOFT CLEAR

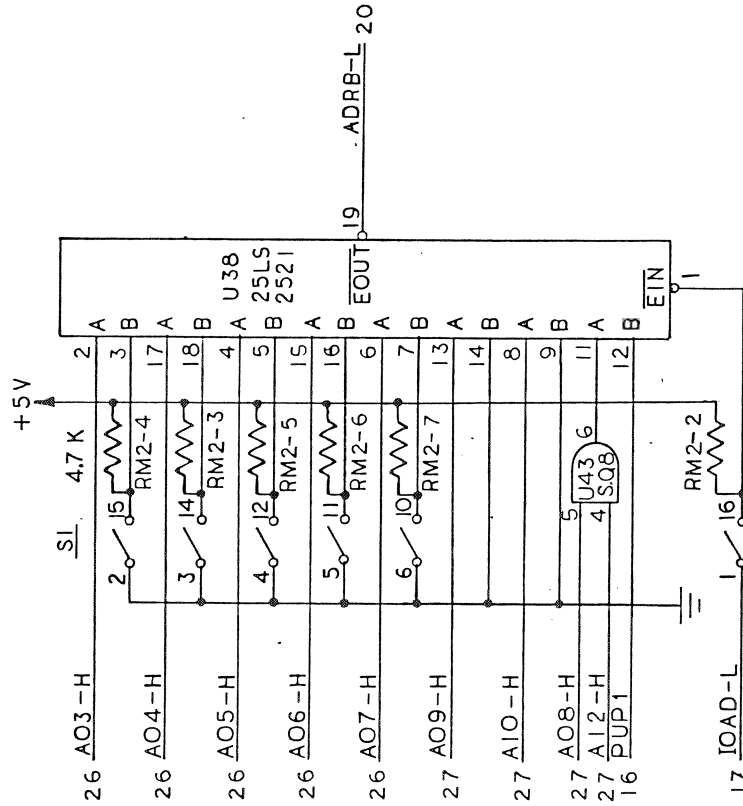


## CLOCKS

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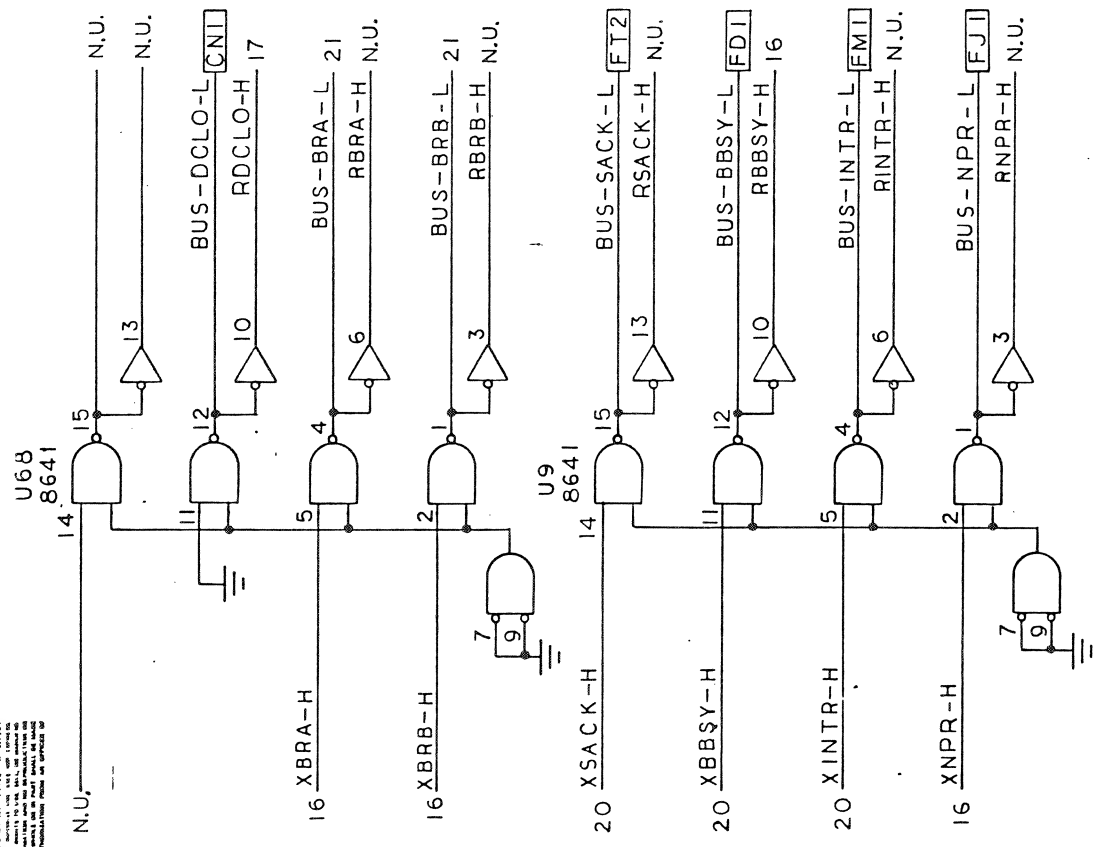


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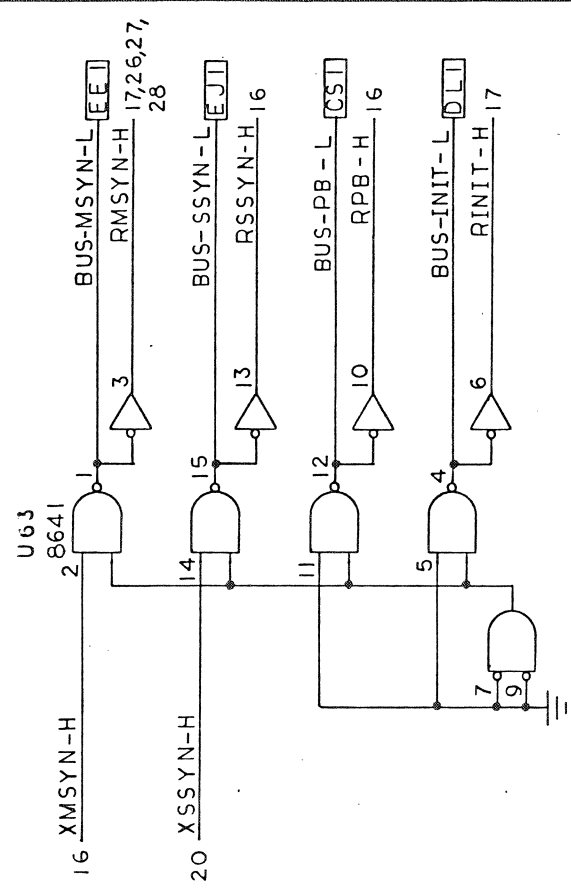


ADDRESS SELECT B

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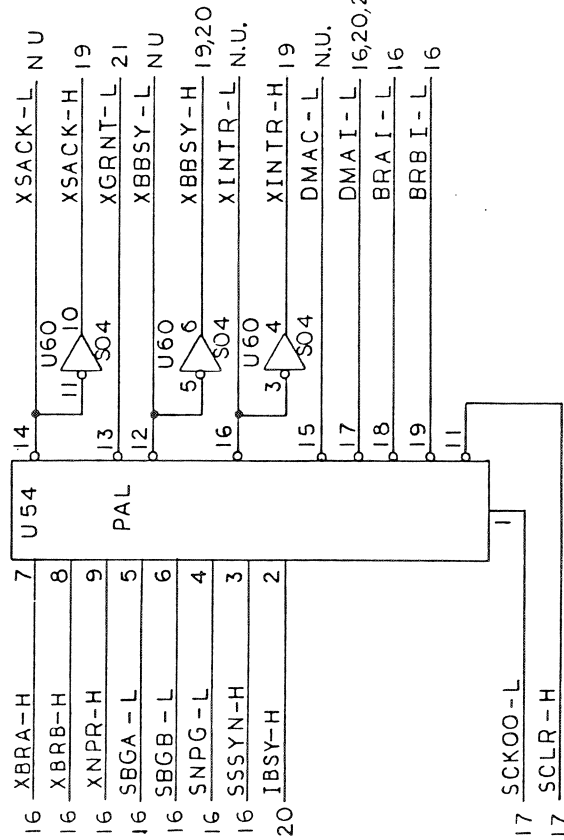


BUS TRANSCIEVERS

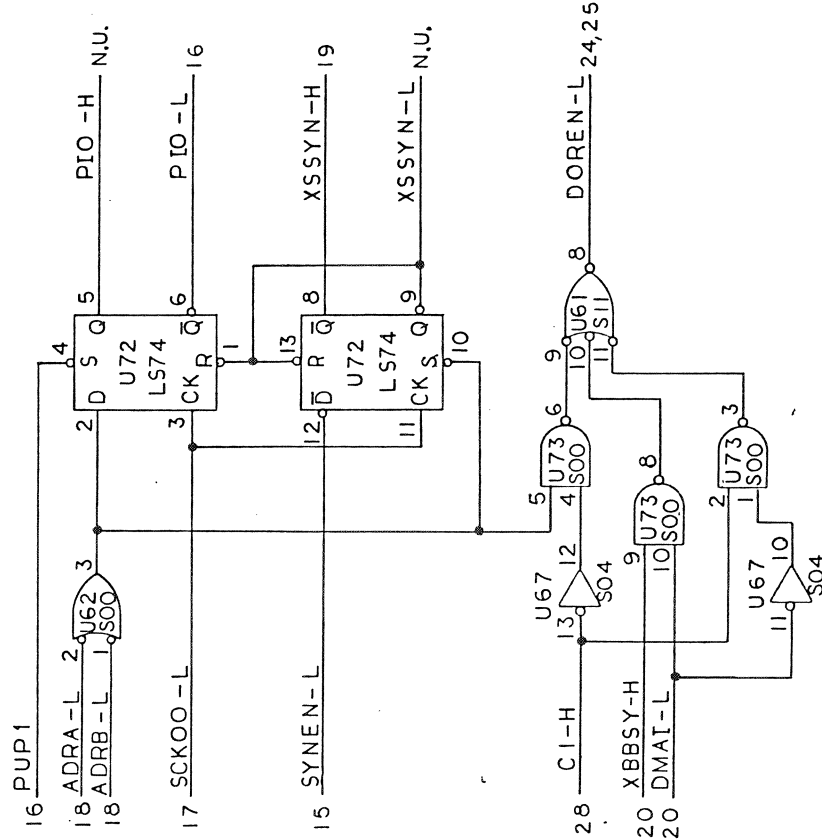


BUS TRANSCIEVERS

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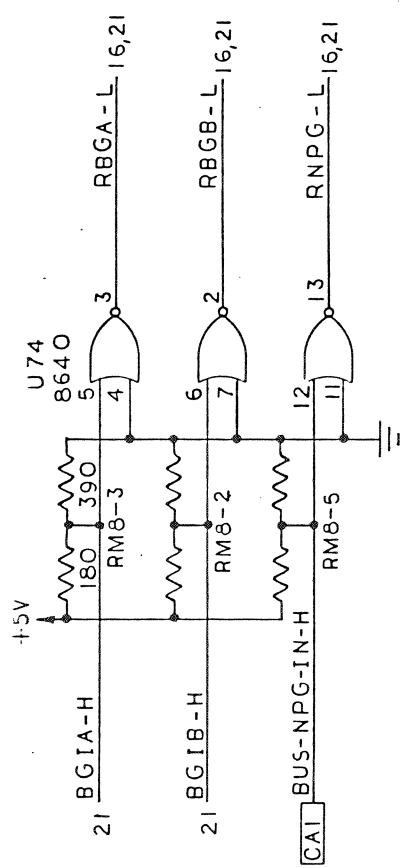
## BUS CONTROLLER



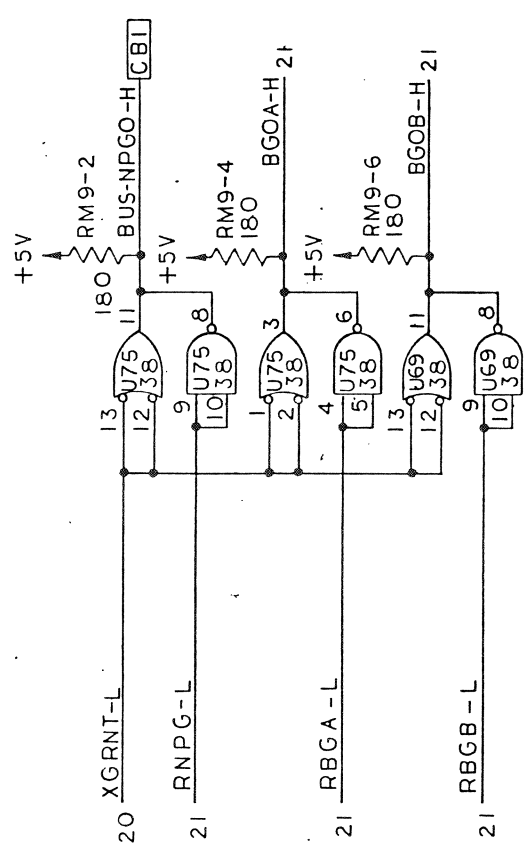
See instruction sheet for details of the interrupt level selection. The interrupt level selection is made by the interrupt level selection switch. The interrupt level selection switch is located on the front panel of the computer. The interrupt level selection switch is labeled "INTERRUPT LEVEL SELECTION". The interrupt level selection switch has four positions: "0", "1", "2", and "3". The interrupt level selection switch is currently in position "0".

21	BGOB-H	10	3	BGIB-H	21
21	BGOA-H	50	7	BGIA-H	21
21	BUS-BG4-IN-H	40	2	BUS-BG4-OUT-H	21
DP2	BG5-IN-H	80	6	BG5-OUT-H	DT2
DM2	BG6-IN-H	90	10	BG6-OUT-H	DN2
DK2	BG7-IN-H	110	12	BUS-BG7-OUT-H	DL2
19	BR8-L	130	14	BUS-BR4-L	DH2
19	BUS-BRA-L	150	16	BR5-L	DF2
			17	BR6-L	DE2
			18	BUS-BR7-L	DD2

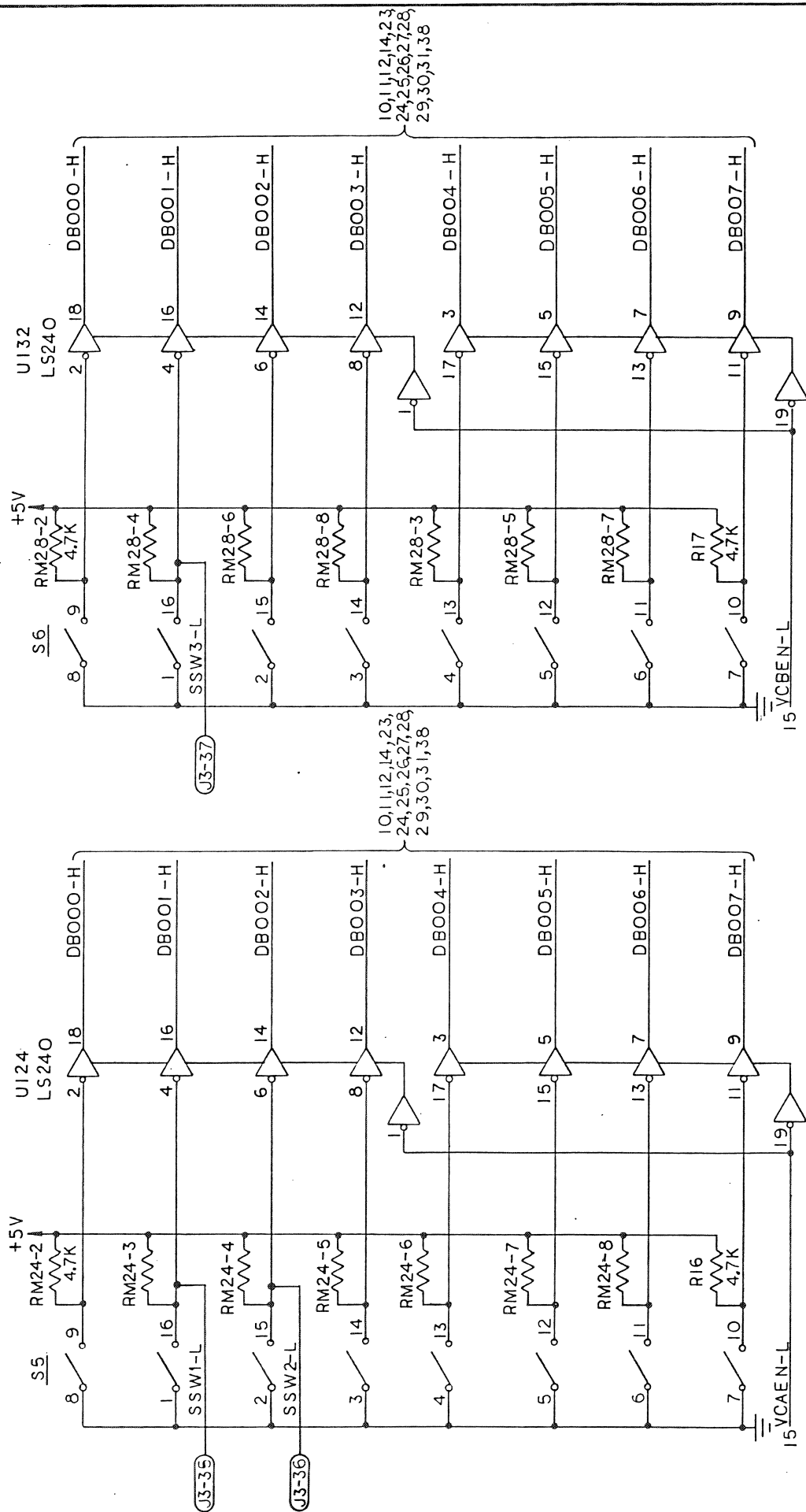
# INTERRUPT LEVEL SELECTION



# GRANT BUS RECEIVERS



# GRANT BUS DRIVERS



# VECTOR A

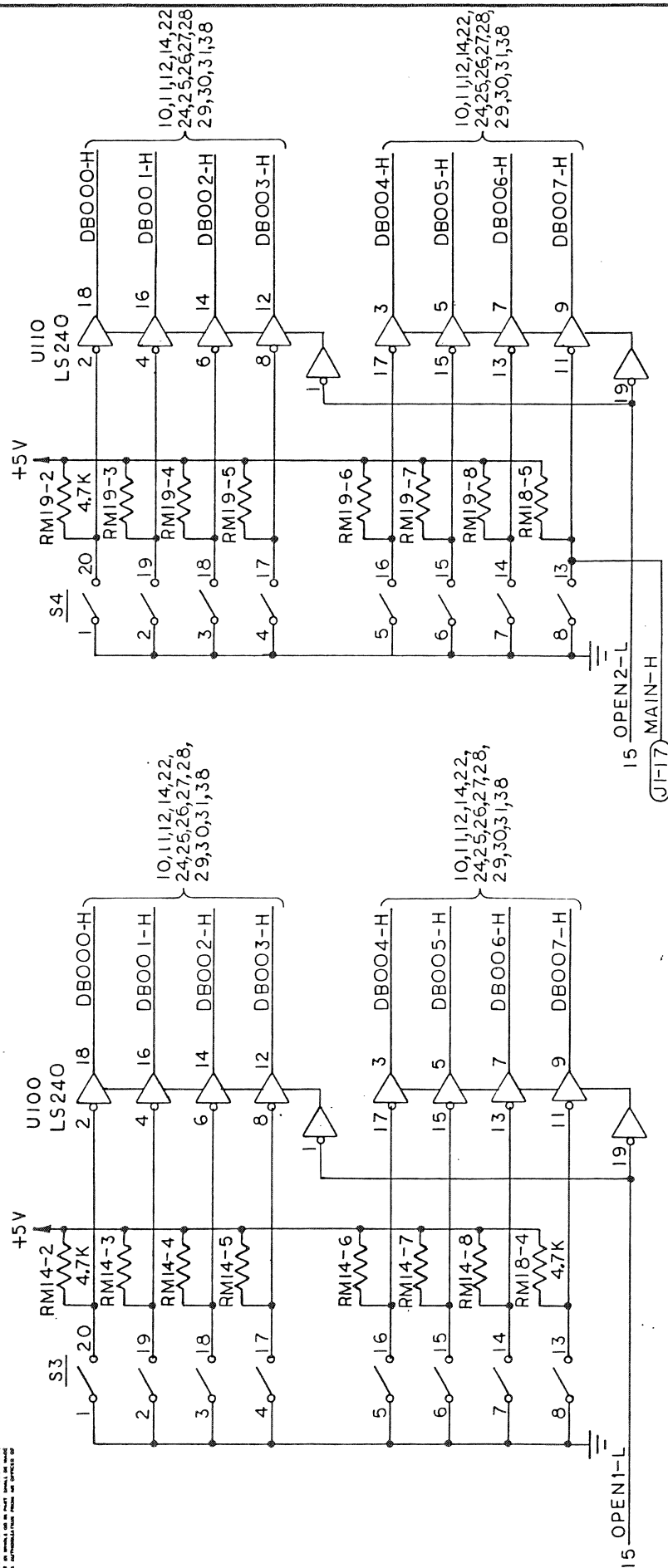
# VECTOR B

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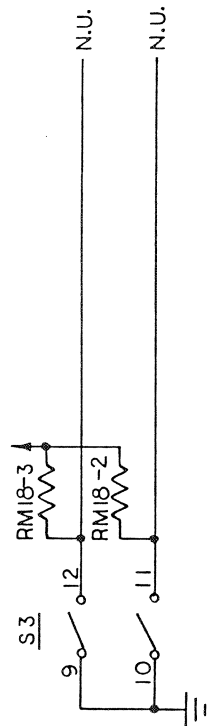
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b. 03003

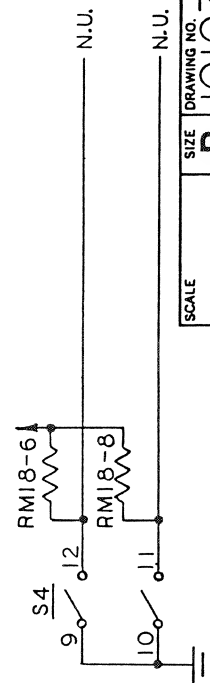
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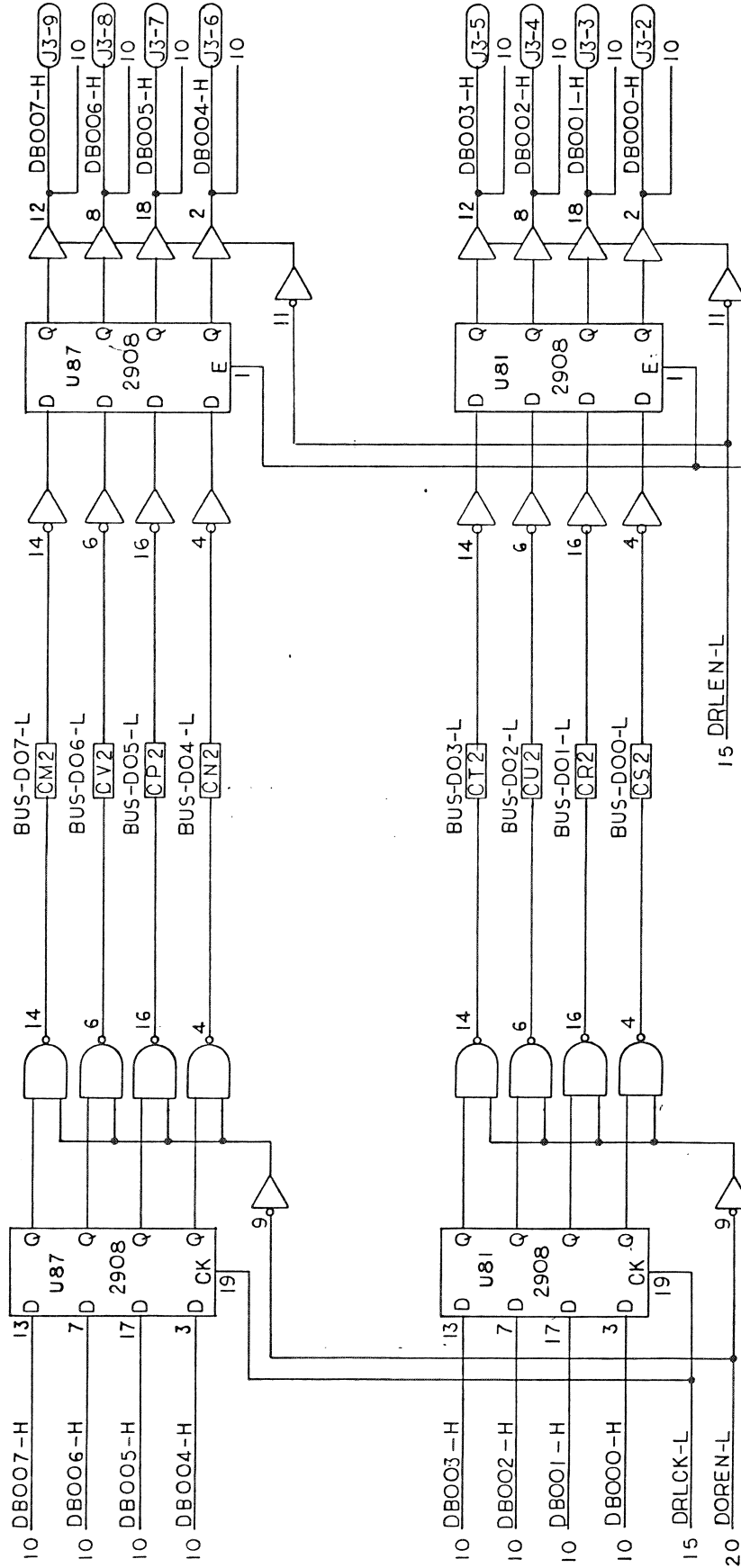
OPTION SWITCHES GROUP 1



OPTION SWITCHES - GROUP 2



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DATA INPUT REGISTER

LOW BYTE

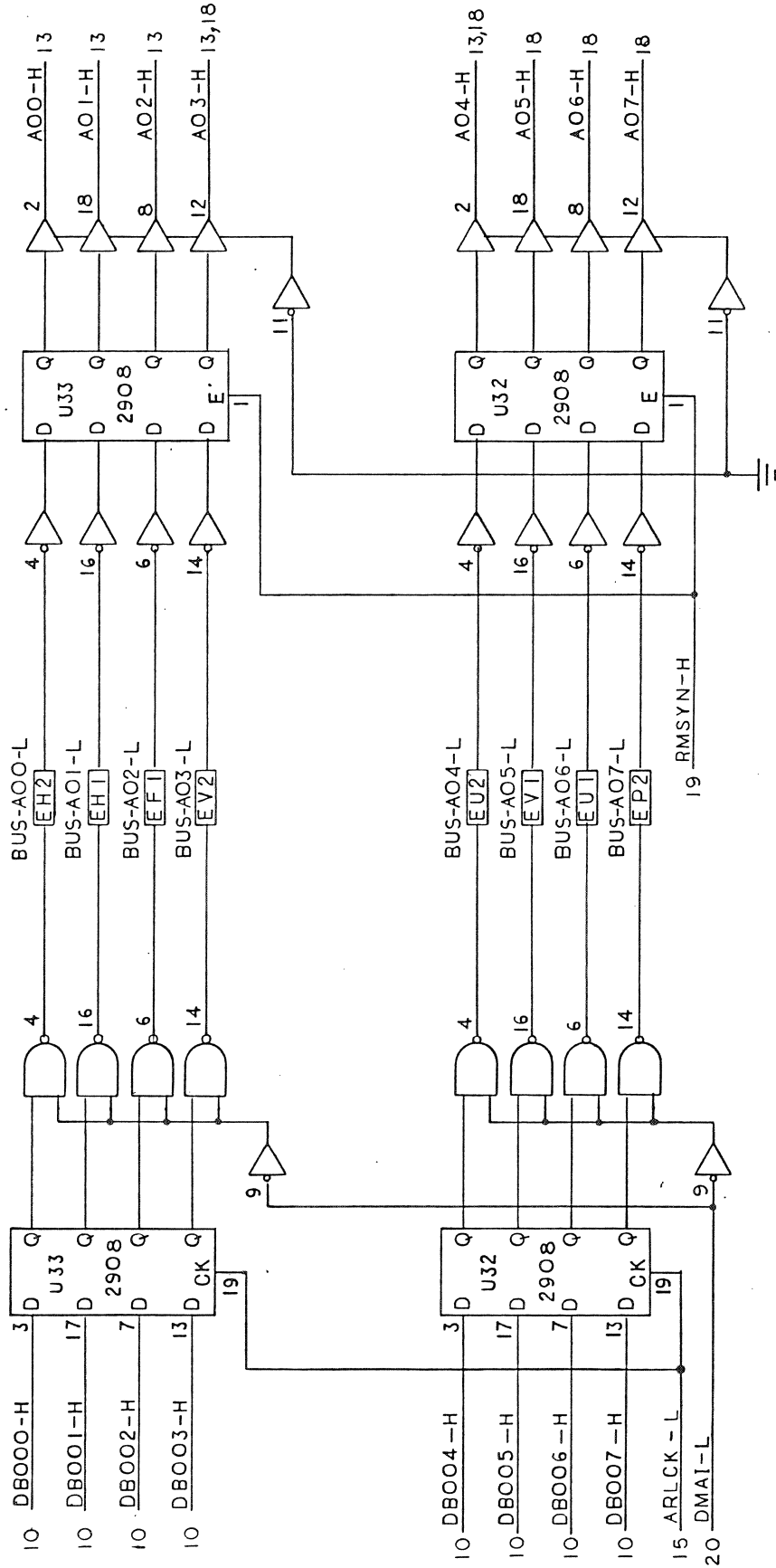
DATA OUTPUT REGISTER

LOW BYTE





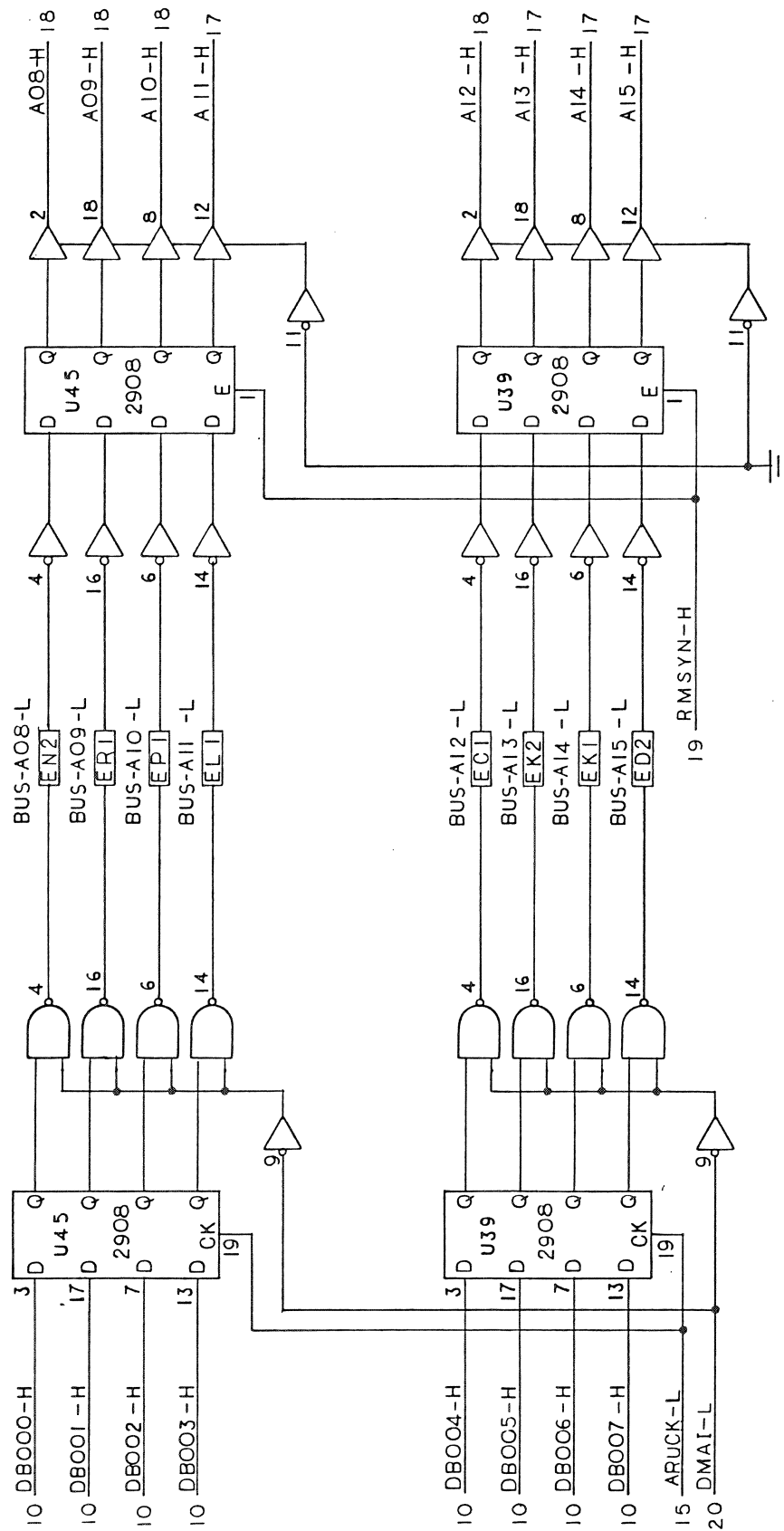
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# ADDRESS INPUT LATCH

# ADDRESS OUTPUT REGISTER

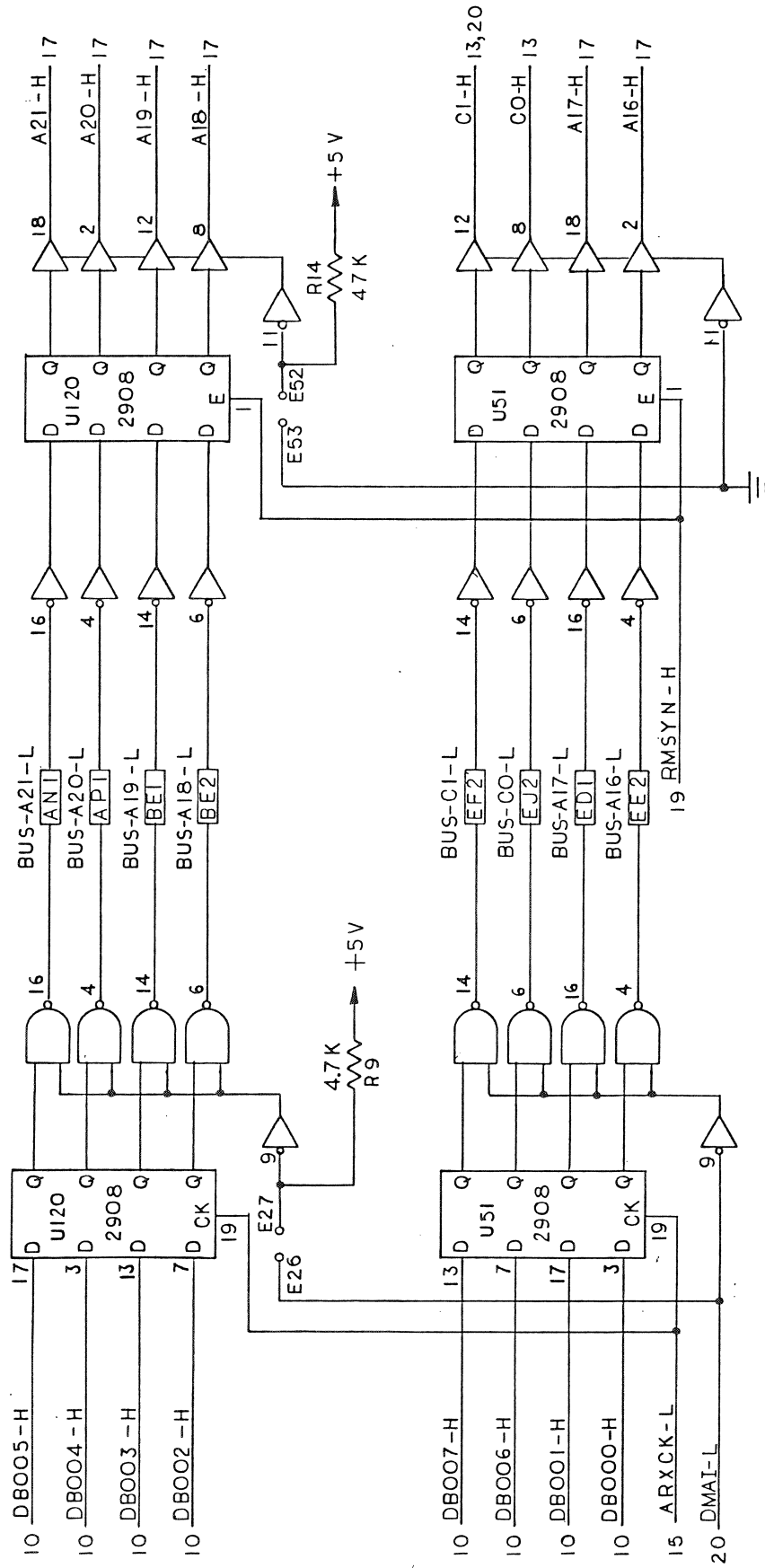
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ADDRESS INPUT LATCH

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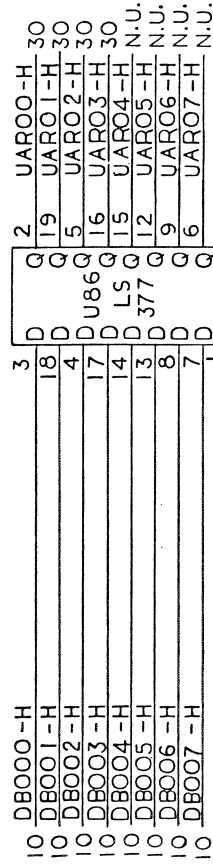


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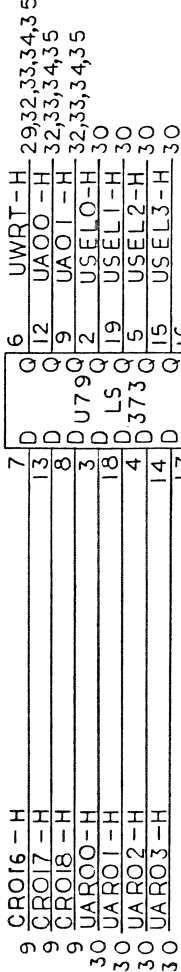
ADDRESS INPUT LATCH

UART INPUT DATA REGISTER

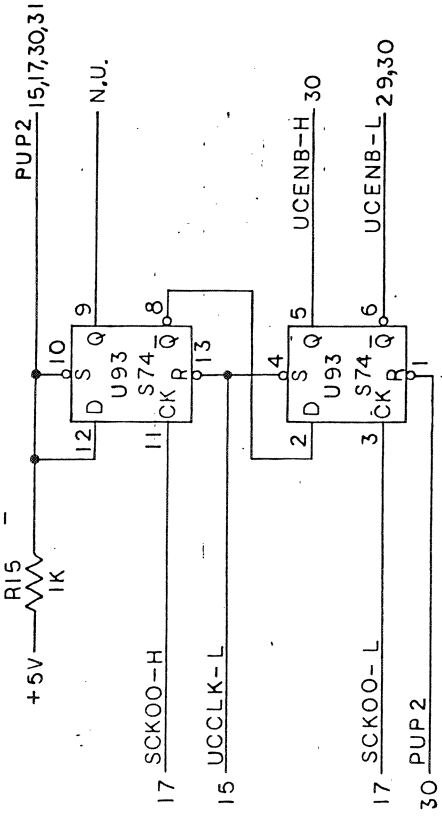
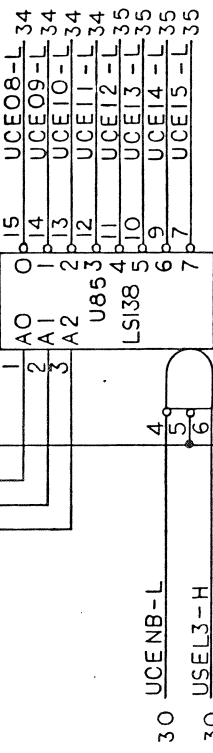
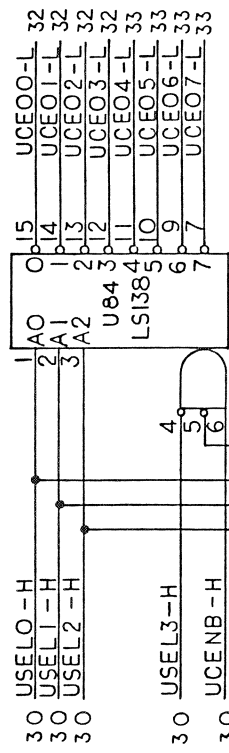
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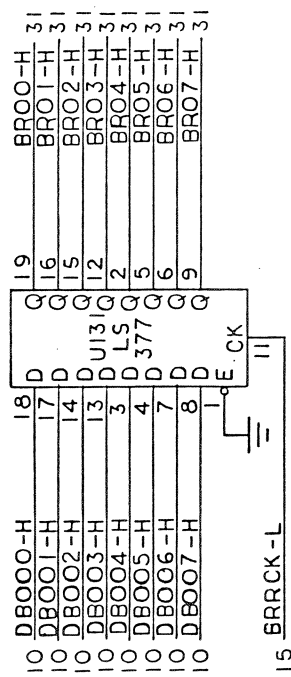
# UART ADDRESS REGISTER



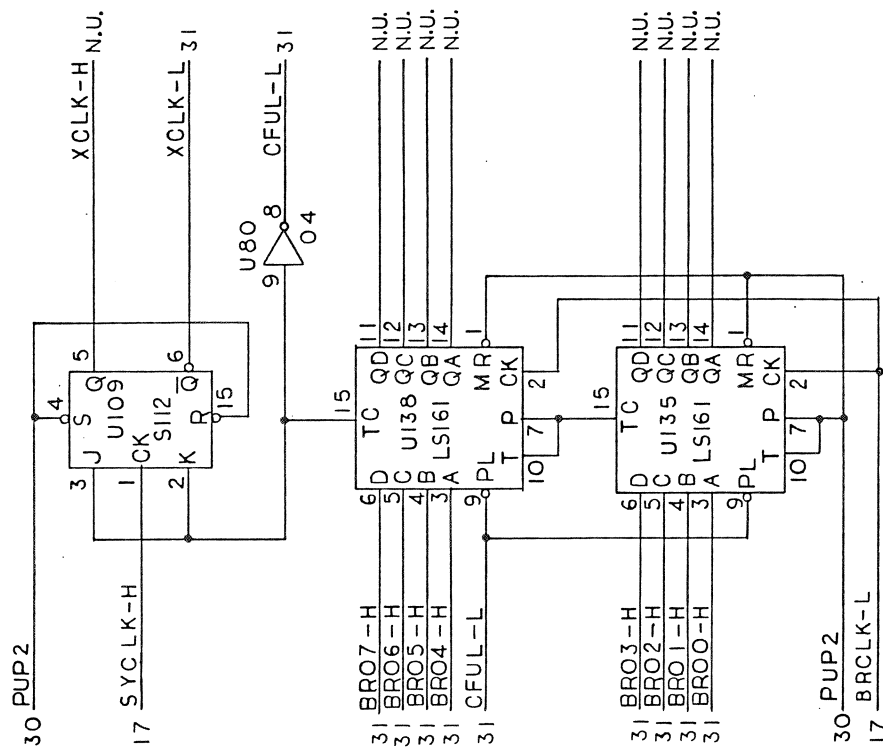
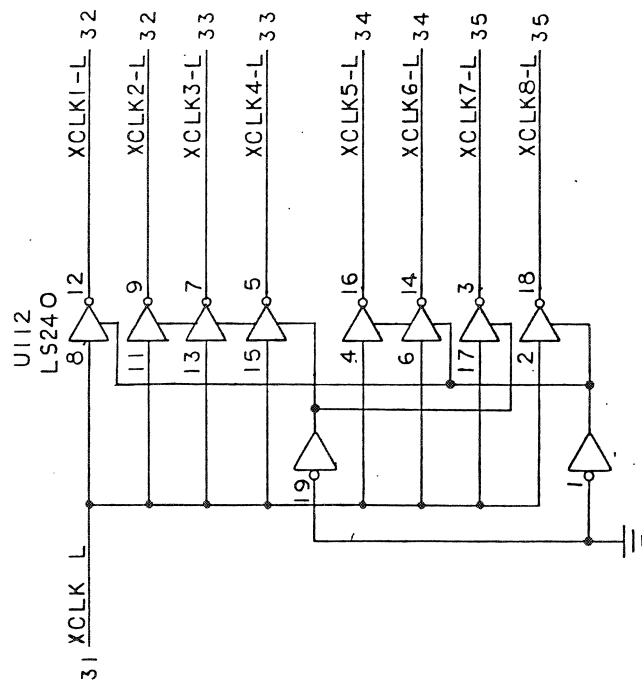
# UART COMMAND DECODE



# UART CHIP ENABLES

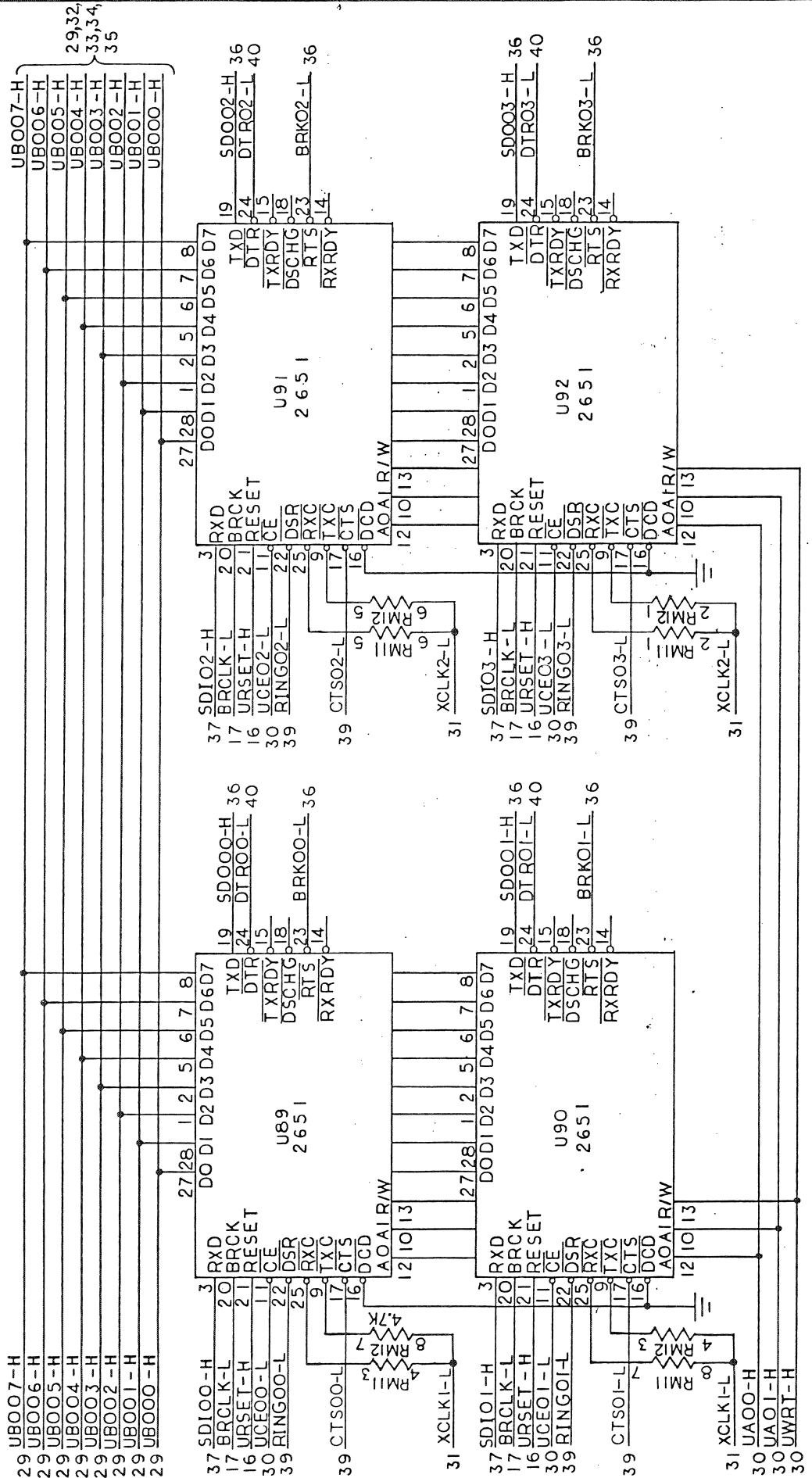


## EXT. BAUD RATE REGISTER



## UART EXT. CLOCK GENERATOR

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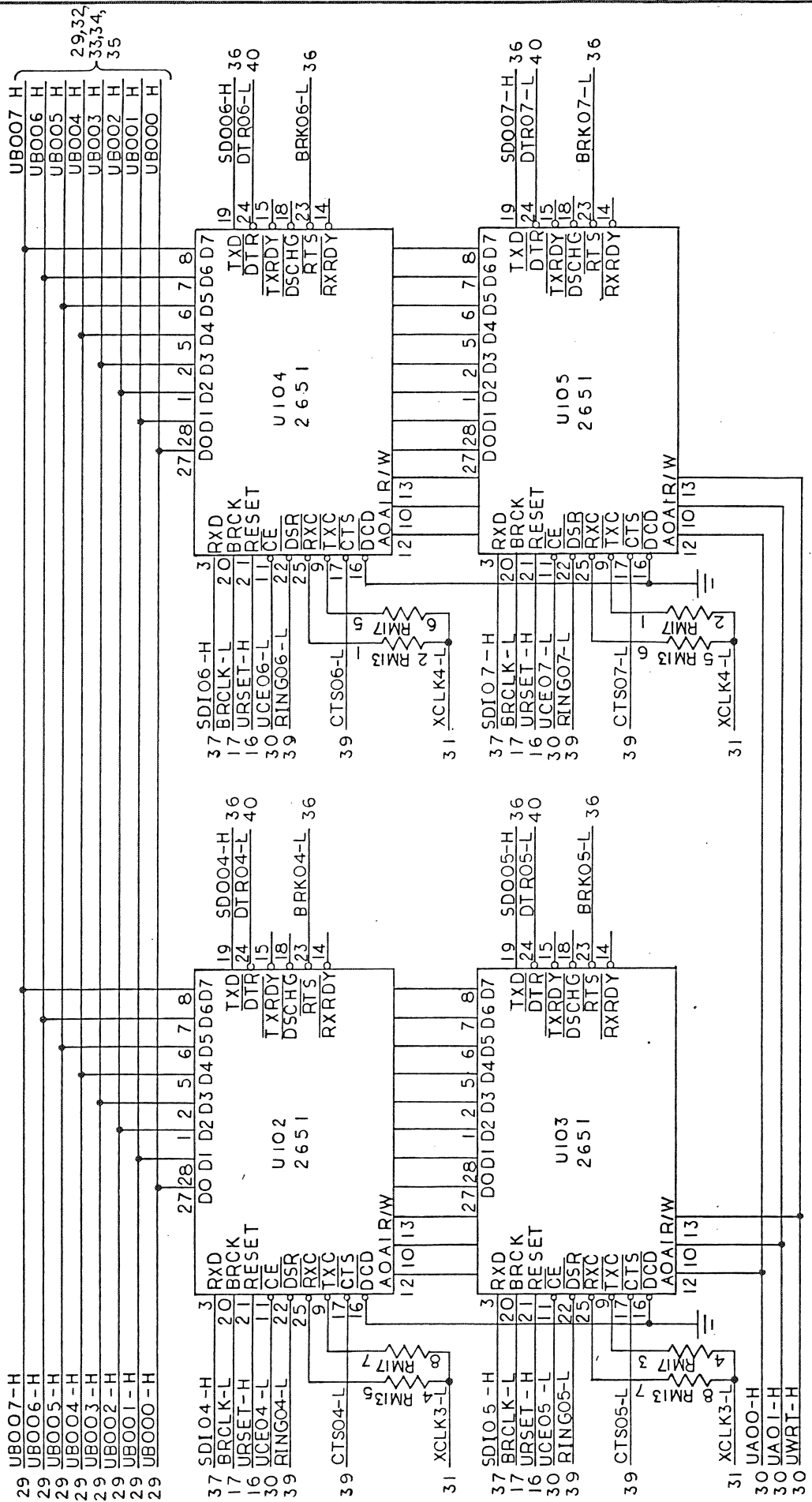


UART CHO AND CHI

UART CH2 AND CH3



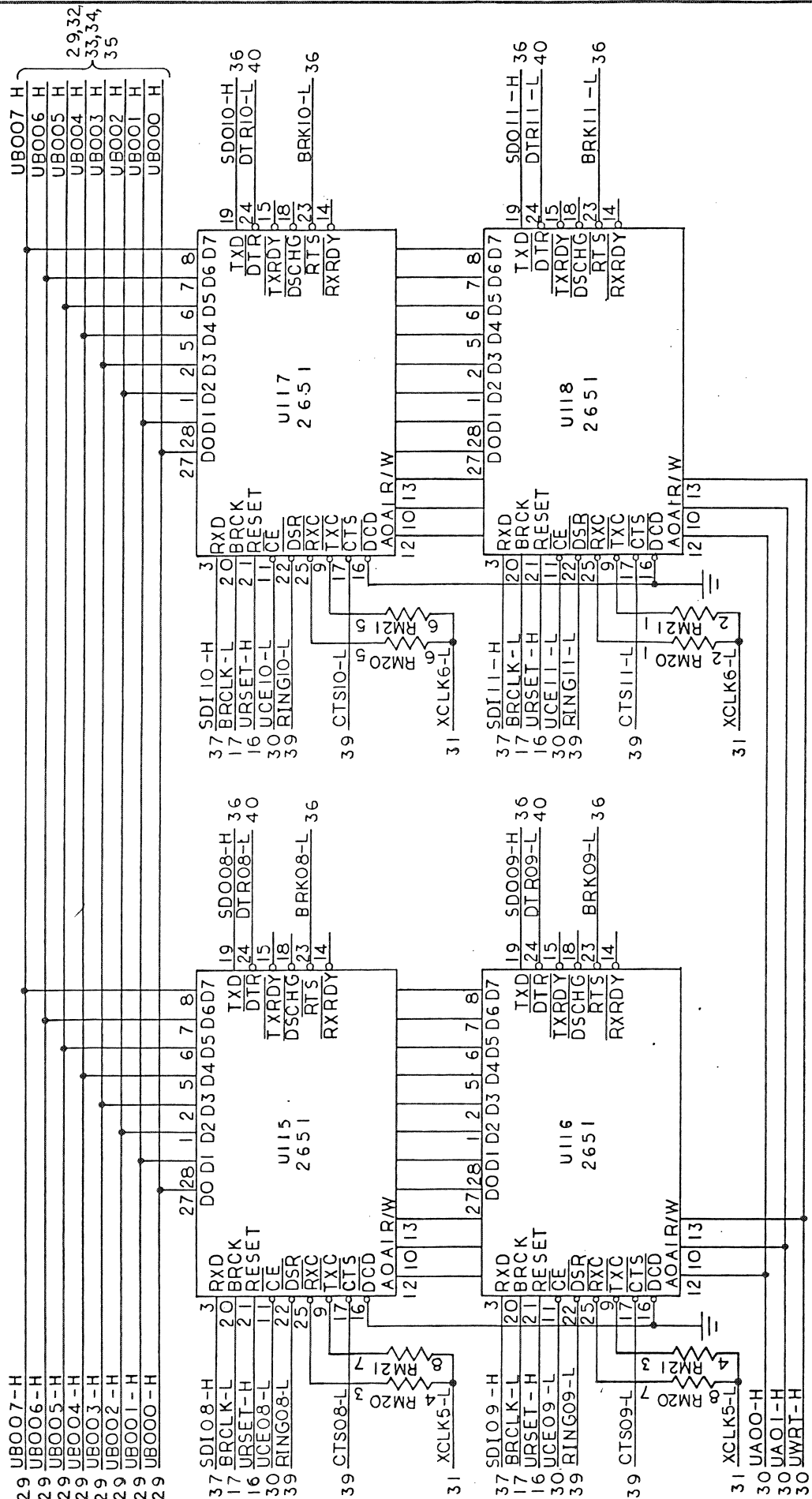
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UART CH4 AND CH5

UART CH6 AND CH7

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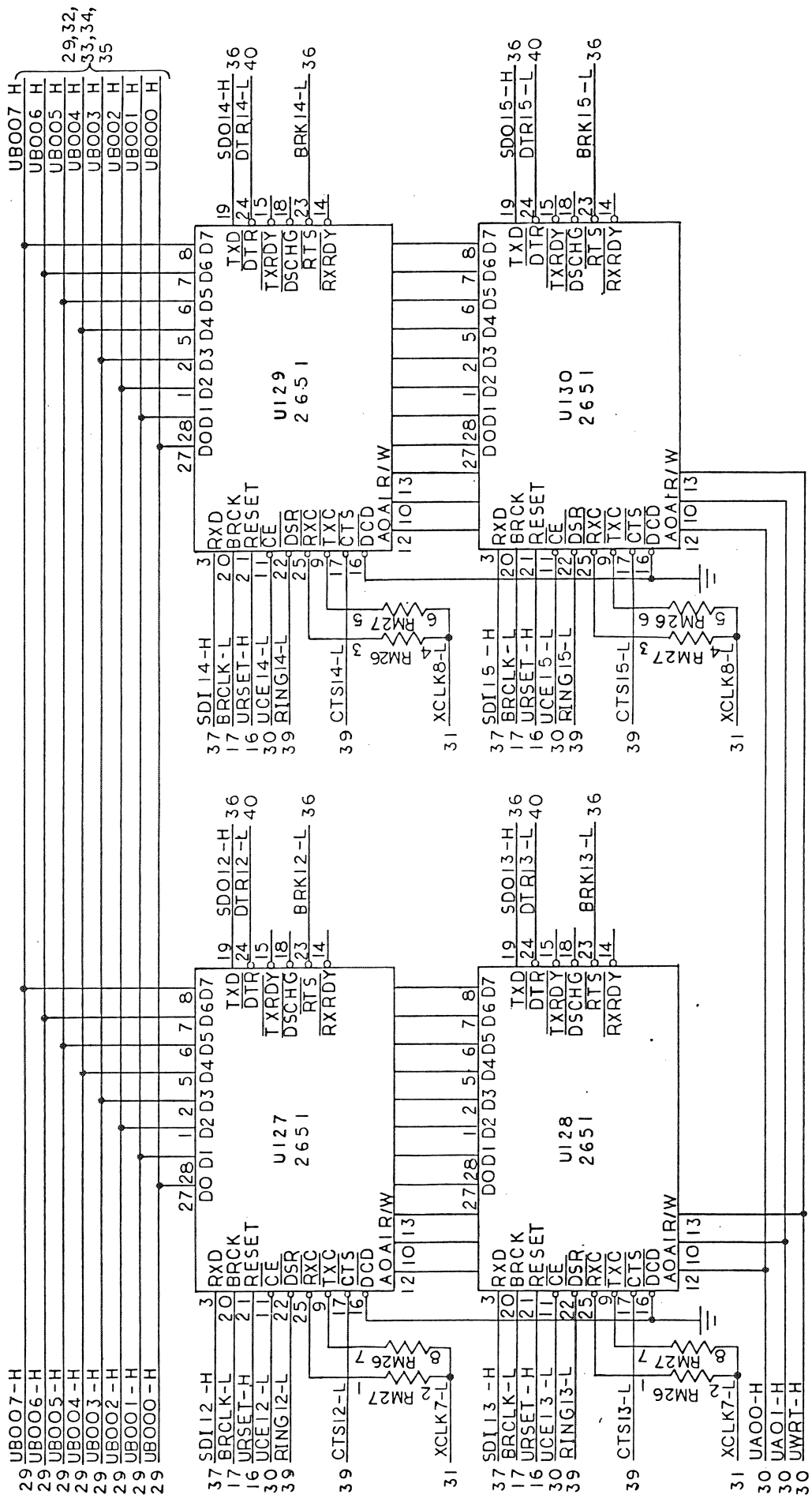


UART CH8 AND CH9

UART CIO AND CH11

SCALE	SIZE	DRAWING NO.	DO NOT SCALE	DRAWING	SHEET
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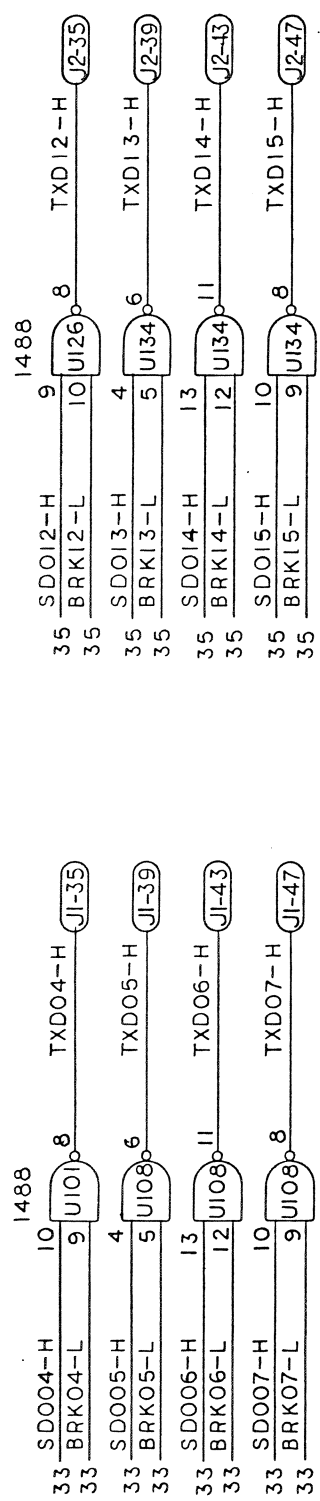
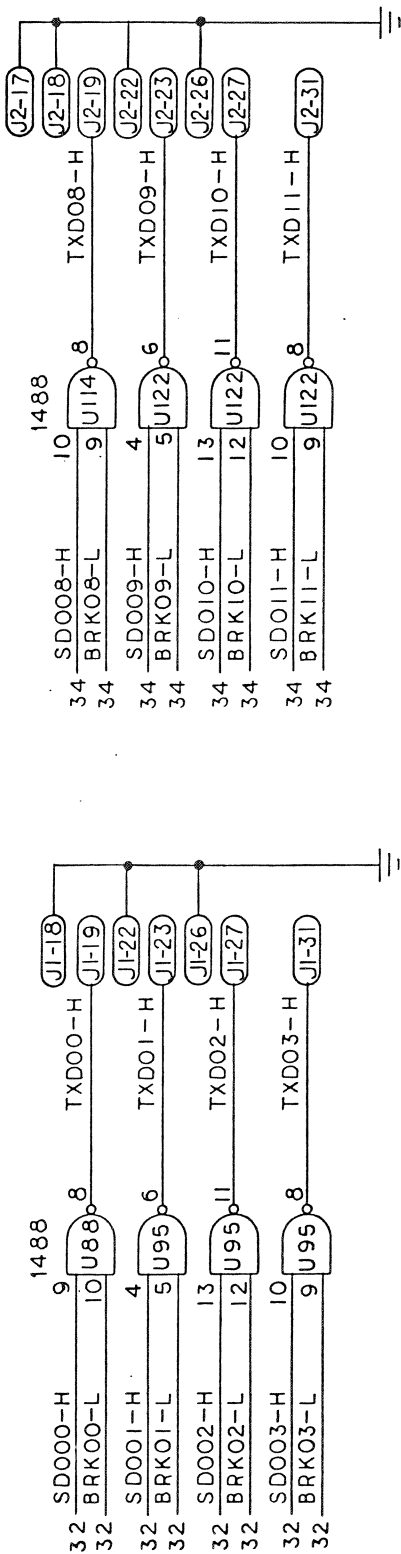


UART CHI2 AND CHI3

UART CHI4 AND CHI5

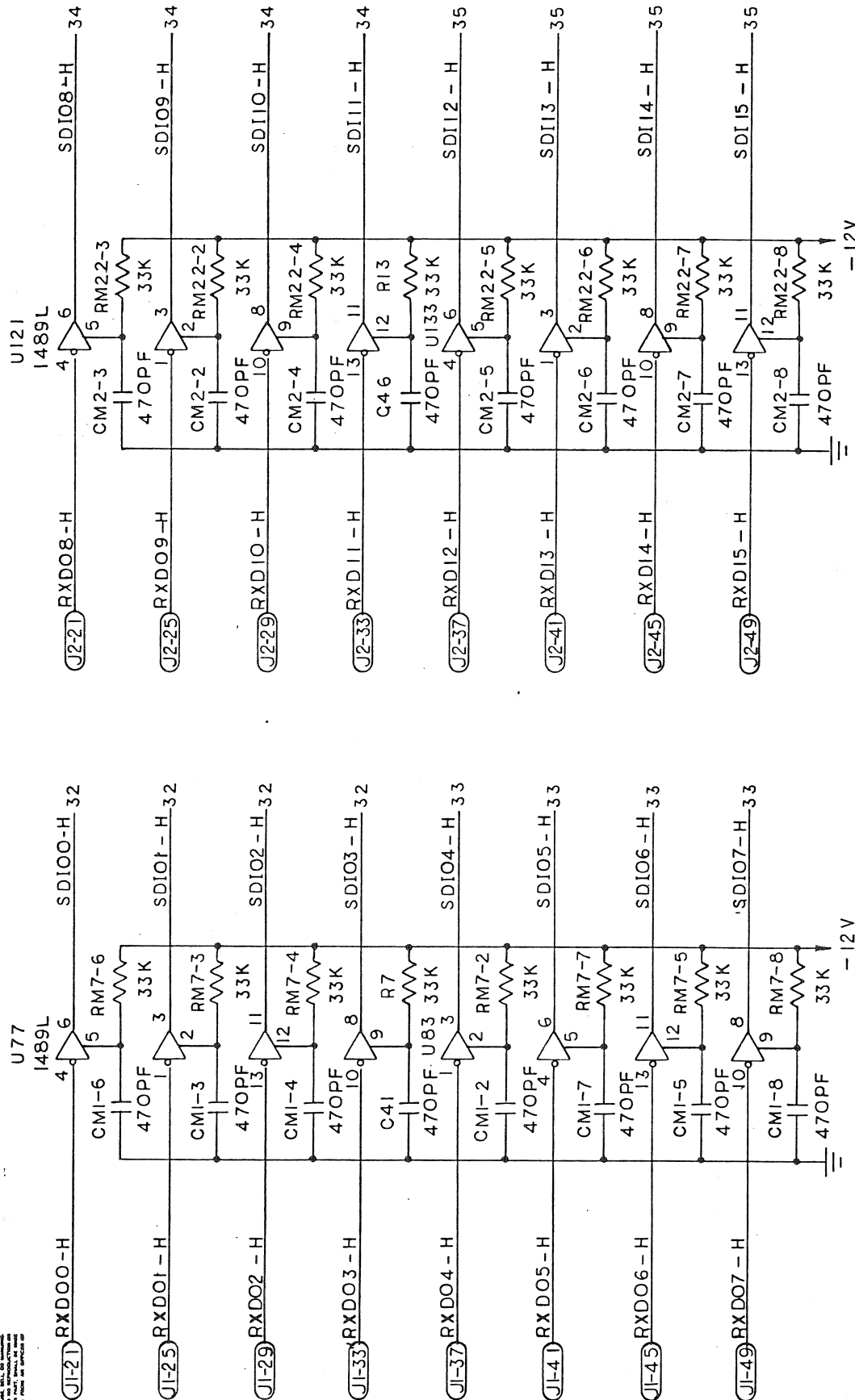
SCALE	SIZE	DRAWING NO.	DO NOT SCALE DRAWING	SHEET
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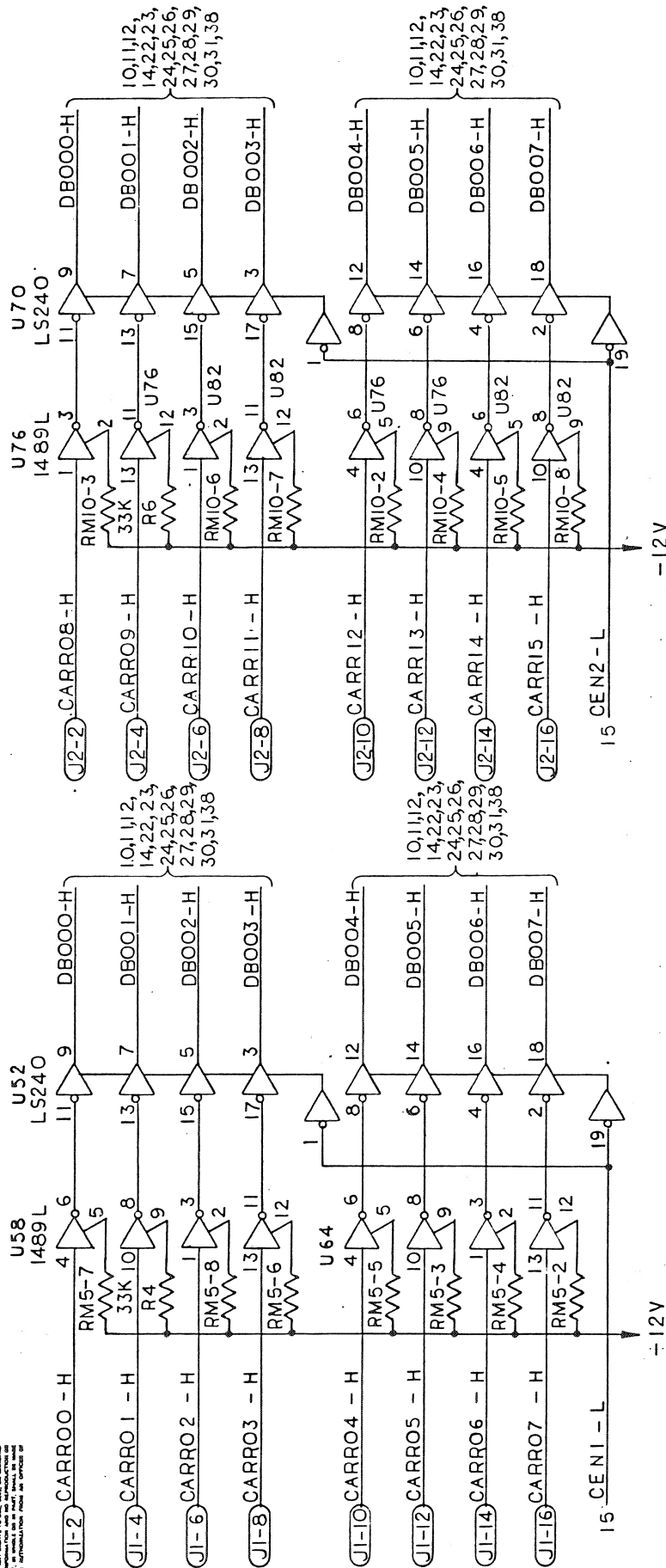


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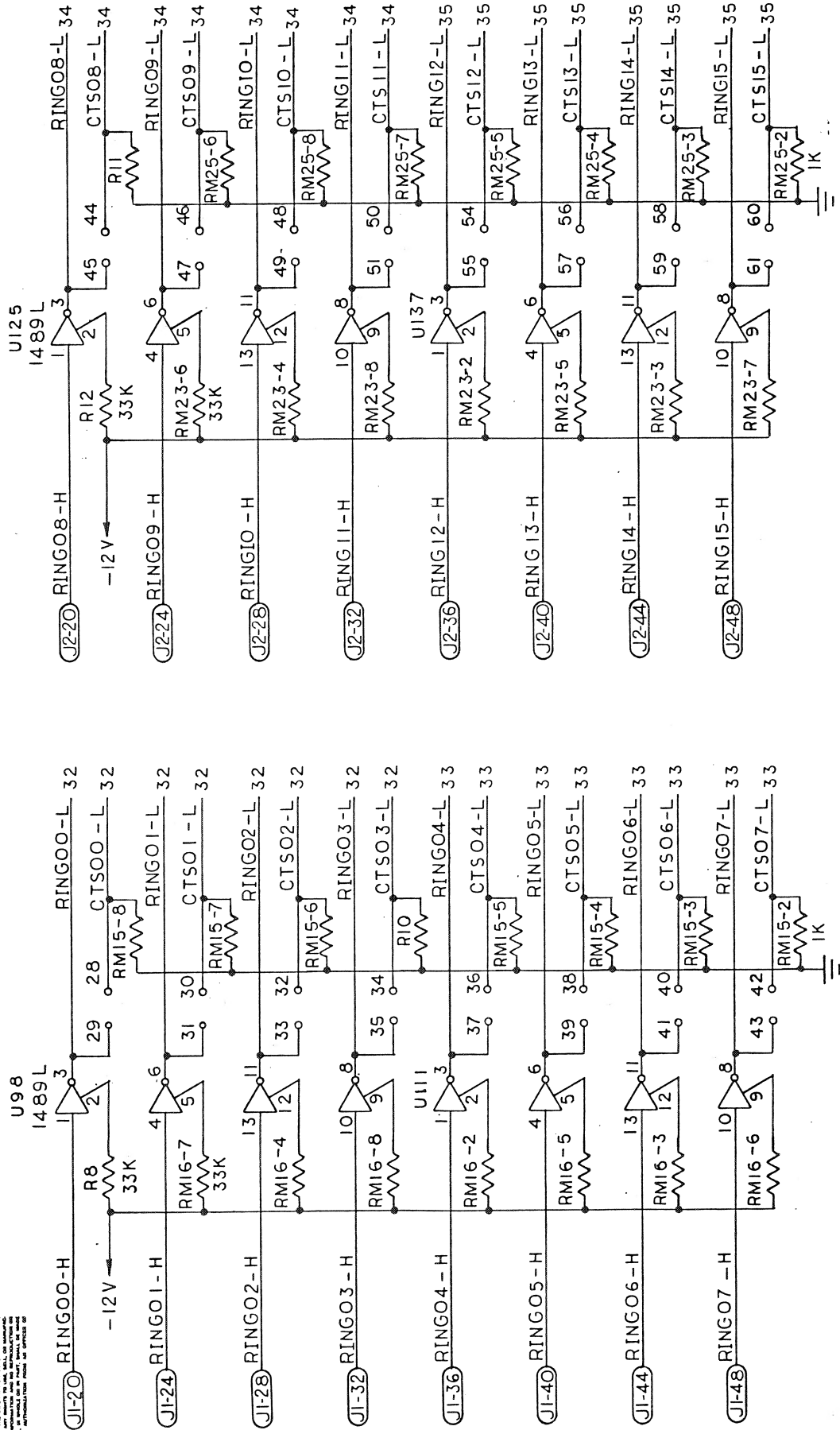


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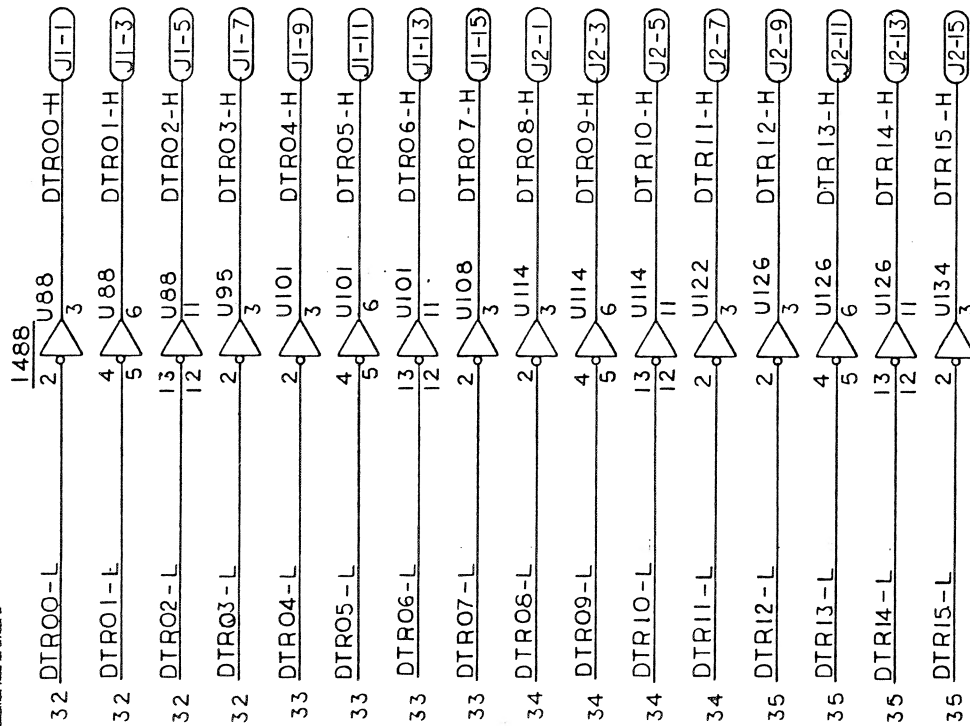
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